IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**8.0**
Revision	Subject
	Discrete Components

1.0 INTRODUCTION

This section covers land patterns for various discrete components. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

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Rectangular Leadless Components

Circular Leadless Components

Small Outline Transistors (SOT) and Diodes (SOD)

Modified Through-Hole (TO) Packs for Transistors and Diodes

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-1 8 mm and 2 mm Taping of Surface Mount Components for Automatic Handling

EIA-481-2 16 mm and 24 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid System for Printed Circuits

3.0 GENERAL INFORMATION

3.1 Packaging Discrete components are generally purchased in 8 mm and 12 mm wide tape and reel. See Figure 1. EIA-481 is the applicable specification for tape and reel. Consult your manufacturers guide for the packaging availability of your component.

Parts susceptible to damage by electrostatic discharge shall be supplied in a manner that prevents such damage. Tape peel strength shall be 40 ±30 grams. Peel from the top for the top cover of the tape. Reel materials used in the construction of the reel shall be easily disposable metal, chip board, styrene plastic or equivalent. Reels shall not cause deterioration of the components or their solderability. Reels must be able to withstand high humidity conditions.

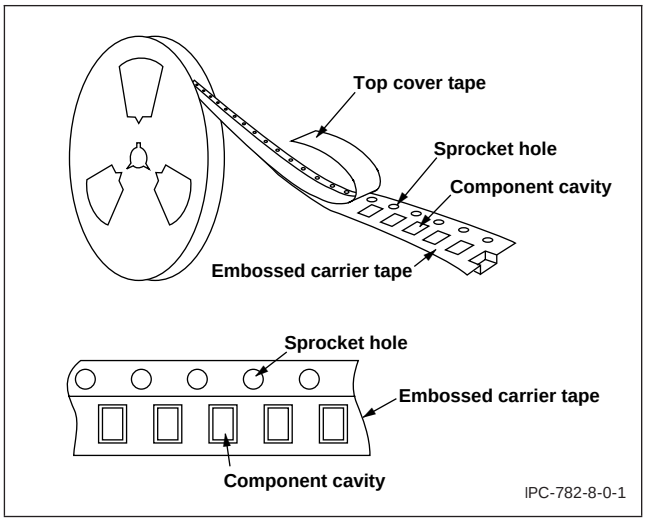

Figure 1 Packaging

3.2 Resistance to Cleaning Processes Parts must be capable of withstanding cleaning processes currently used by board assembly manufacturers. This may include as a minimum 4-minute exposures to solvent cleaning solutions at 40°C, plus a minimum of a 1-minute exposure to ultrasonic immersion at a frequency of 40 kHz and a power of 100 watts per square foot. Alkaline systems in use shall also not damage parts or remove markings.

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1. Application for copies should be addressed to EIA, 2001 Pennsylvania Ave N.W., Washington, DC, 20006-1813 or Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131—1211 Geneva 20, Switzerland

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as chip resistors.

This subsection provides the component and land pattern dimensions for chip resistors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the chip resistor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for resistors. The following sections describe the most common types.

3.1 Basic Construction The resistive material is applied to a ceramic substrate and terminated symmetrically at both ends with a ''wrap around'' metal U-shaped band. The resistive material is face-up, thus trimming to close tolerances is possible. Since most equipment uses a vacuum-type pickup head, it is important that the surface of the resistor is made flat after trimming, otherwise vacuum pickup might be difficult. See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in.] thick.

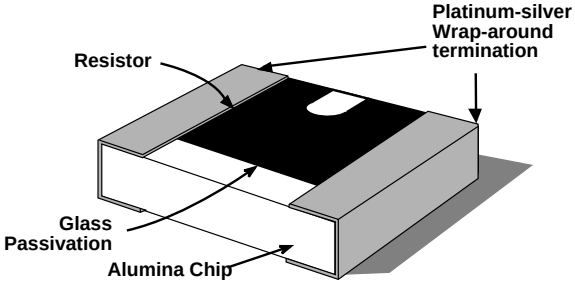
The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metalization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Resistors equal to or larger than 2012 [0805] are labeled. Resistors smaller than 1608 [0603] are generally unlabeled.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.



Wire Bond Construction

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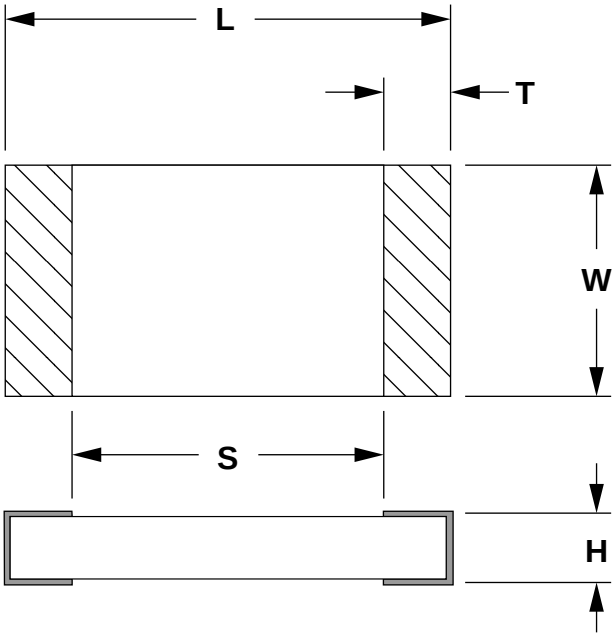
Figure 1 Chip resistor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for chip resistors.



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mm [in] Component Identifier	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	1.00	1.10	0.40	0.70	0.48	0.60	0.10	0.30	0.40
1608 [0603]	1.50	1.70	0.70	1.11	0.70	0.95	0.15	0.40	0.60
2012 [0805]	1.85	2.15	0.55	1.32	1.10	1.40	0.15	0.65	0.65
3216 [1206]	3.05	3.35	1.55	2.32	1.45	1.75	0.25	0.75	0.71
3225 [1210]	3.05	3.35	1.55	2.32	2.34	2.64	0.25	0.75	0.71
5025 [2010]	4.85	5.15	3.15	3.92	2.35	2.65	0.35	0.85	0.71
6332 [2512]	6.15	6.45	4.45	5.22	3.05	3.35	0.35	0.85	0.71

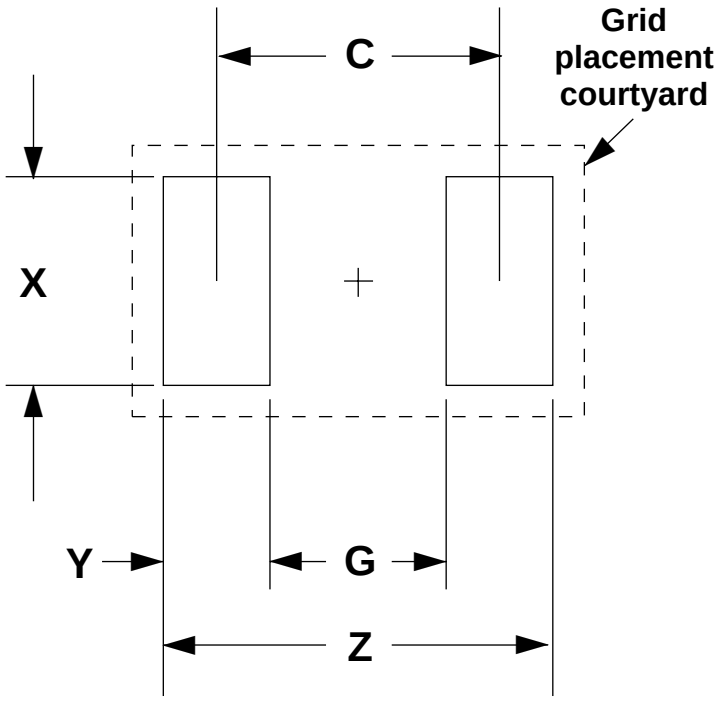
Figure 2 Chip resistor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for chip resistors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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RLP No.	Component Identifier (mm) [in.]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
100A	1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
101A	1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
102A	2012 [0805]*	3.20	0.60	1.50	1.30	1.90	4x8
103A	3216 [1206]*	4.40	1.20	1.80	1.60	2.80	4x10
104A	3225 [1210]*	4.40	1.20	2.70	1.60	2.80	6x10
105A	5025 [2010]*	6.20	2.60	2.70	1.80	4.40	6x14
106A	6332 [2512]*	7.40	3.80	3.20	1.80	5.60	8x16

**Note:* If a more robust pattern is desired for wave soldering devices larger than 1608 [0603], add 0.2 mm to the Y-dimension, and consider reducing the X-dimension by 30%. Add a ''W'' suffix to the number; e.g., 103W.

Figure 3 Chip resistor land pattern dimensions

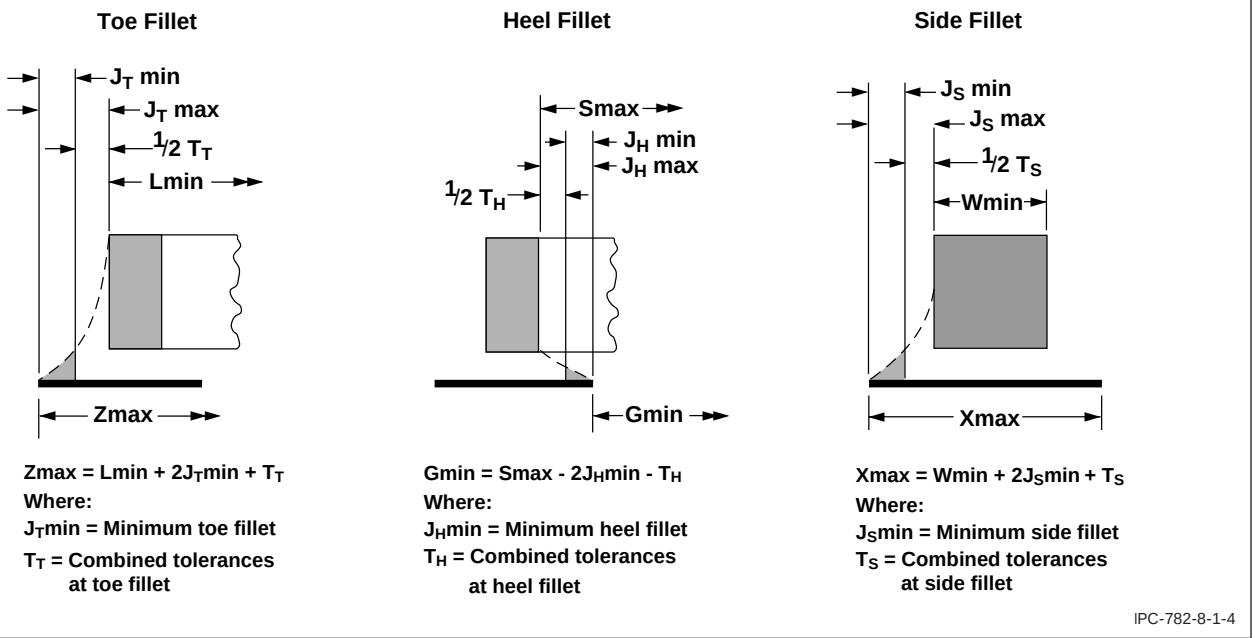
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed, and are given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions.)

The dimensions for the statistical minimum and maximum solder joint fillets at the toe, heel, or side (J_T, J_H, or J_S) have been determined based on the equations detailed in Section 3.3. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



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RLP No.	Tolerance (mm) Assumptions		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	J_{Tmin}	J_{Tmax}	C_S	J_{Hmin}	J_{Hmax}	C_W	J_{Smin}	J_{Smax}
100A	0.10	0.10	0.10	0.51	0.60	0.30	–0.02	0.15	0.12	0.02	0.11
101A	0.10	0.10	0.20	0.53	0.65	0.41	0.04	0.25	0.25	0.01	0.15
102A	0.10	0.10	0.30	0.51	0.68	0.77	–0.03	0.36	0.30	0.03	0.20
103A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
104A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
105A	0.10	0.10	0.30	0.51	0.68	0.77	0.27	0.66	0.30	0.01	0.18
106A	0.10	0.10	0.30	0.46	0.63	0.77	0.32	0.71	0.30	–0.09	0.08

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as chip capacitors.

This subsection provides the component and land pattern dimensions for chip capacitors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the chip capacitor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for capacitors. The following sections describe the most common types.

3.1 Basic Construction Multilayer ceramic capacitors use substrate materials such as alumina for hybrid circuits and porcelainized metal. The monolithic construction used in producing these chips results in a solid block of ceramic with an enclosed electrode system and metallized ends for circuit attachment. This solid block is rugged and capable of withstanding the harsh environment and treatment associated with manufacturing processes. See Figure 1.

Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consecutive drying and firing eliminates the organic components and effects a bond between the ceramic dielectric and glass constituent in the termination.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Ceramic capacitors are typically unmarked.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

Caution should be exercised when using the 4564 (1825) capacitor mounted on organic substrates due to CTE mismatch if the assembly sees wide temperature swings in the assembly process or end use.

1. Termination
2. Dielectric
3. Electrode
4. Chip length
5. "A" electrode print
6. Electrode print
7. Cap (Topping layer)
8. End margin
9. Base layer
10. Shim (Active dielectric layer)
11. Side margin
12. Chip thickness
13. Chip width
14. Termination width

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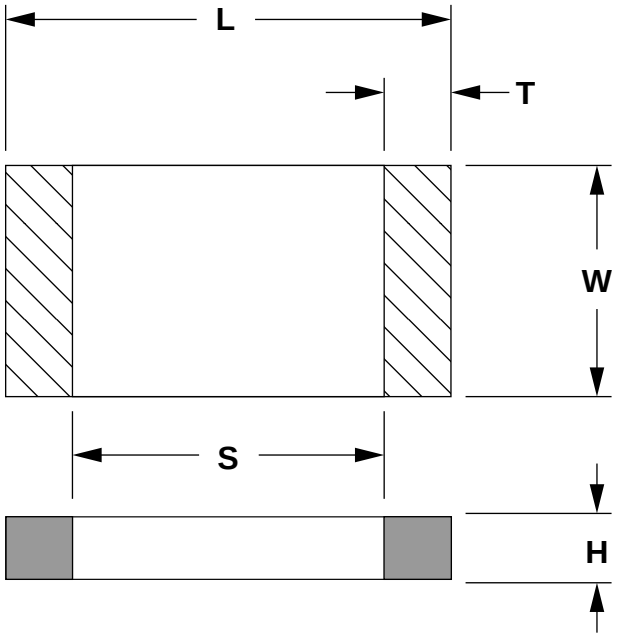
Figure 1 Chip capacitor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for chip capacitors.



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Component Identifier (mm) [in]	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	0.90	1.10	0.30	0.65	0.40	0.60	0.10	0.30	0.60
1310 [0504]	1.02	1.32	0.26	0.72	0.77	1.27	0.13	0.38	1.02
1608 [0603]	1.45	1.75	0.45	0.97	0.65	0.95	0.20	0.50	0.85
2012 [0805]	1.80	2.20	0.30	1.11	1.05	1.45	0.25	0.75	1.10
3216 [1206]	3.00	3.40	1.50	2.31	1.40	1.80	0.25	0.75	1.35
3225 [1210]	3.00	3.40	1.50	2.31	2.30	2.70	0.25	0.75	1.35
4532 [1812]	4.20	4.80	2.30	3.46	3.00	3.40	0.25	0.95	1.35
4564 [1825]	4.20	4.80	2.30	3.46	6.00	6.80	0.25	0.95	1.10

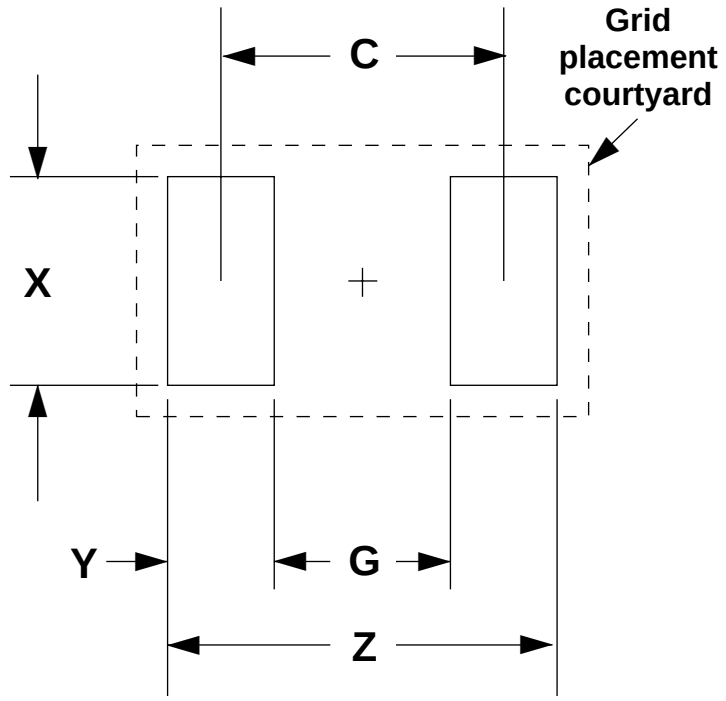
Figure 2 Chip capacitor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for chip capacitors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm) [in]	Z (mm)	G (mm)	X (mm)	Y ref	C ref	Placement Grid (No. of Grid elements)
130A	1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
131A	1310 [0504]	2.40	0.40	1.30	1.00	1.40	4x6
132A	1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
133A	2012 [0805]	3.20	0.60	1.50	1.30	1.90	4x8
134A	3216 [1206]	4.40	1.20	1.80	1.60	2.80	4x10
135A	3225 [1210]	4.40	1.20	2.70	1.60	2.80	6x10
136A	4532 [1812]	5.80	2.00	3.40	1.90	3.90	8x12
137A	4564 [1825]	5.80	2.00	6.80	1.90	3.90	14x12

Figure 3 Chip capacitor land pattern dimensions

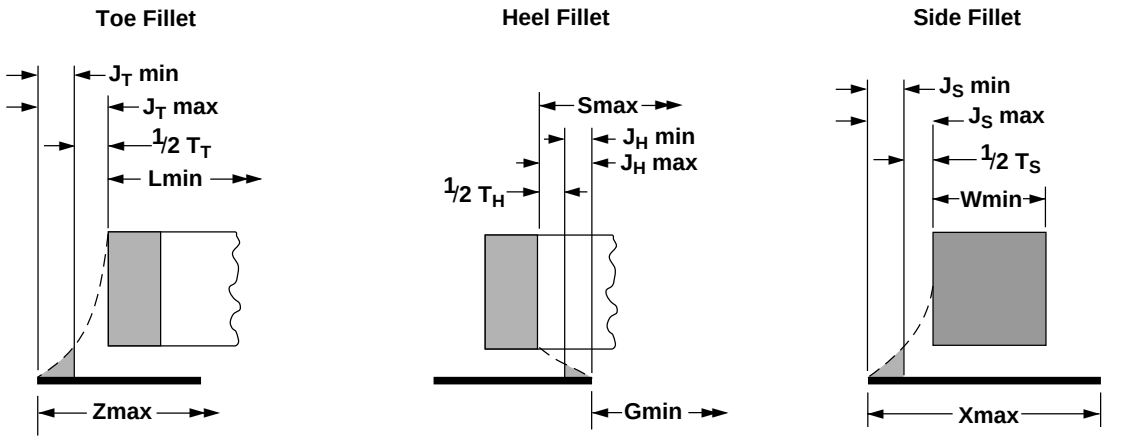
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2$J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - 2$J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + 2$J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	J_{Tmin}	J_{Tmax}	C_s	J_{Hmin}	J_{Hmax}	C_W	J_{Smin}	J_{Smax}
130A	0.10	0.10	0.20	0.53	0.65	0.60	–0.06	0.12	0.20	0.03	0.15
131A	0.10	0.10	0.30	0.52	0.69	1.00	–0.08	0.16	0.50	0.01	0.27
132A	0.10	0.10	0.30	0.51	0.68	0.65	–0.08	0.18	0.30	0.01	0.18
133A	0.10	0.10	0.40	0.49	0.70	0.95	–0.16	0.26	0.40	0.01	0.23
134A	0.10	0.10	0.40	0.49	0.70	1.40	0.14	0.56	0.40	–0.01	0.20
135A	0.10	0.10	0.40	0.49	0.70	1.40	0.14	0.56	0.40	–0.01	0.20
136A	0.10	0.10	0.60	0.49	0.80	1.10	0.15	0.73	0.40	–0.01	0.20
137A	0.10	0.10	0.60	0.49	0.80	1.10	0.15	0.73	0.80	–0.01	0.40

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as inductors.

This subsection provides the component and land pattern dimensions for inductors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the inductor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for inductors. The following sections describe the most common types.

3.1 Basic Construction At the time of publication, there was no industry standard document for leadless inductors. The dimensions were taken from manufacturer's catalogs, but only when at least two component vendors manufacture the same package. However, the same inductor value may not be available in the same package from the two manufacturers. See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Parts are available with or without marked inductance values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

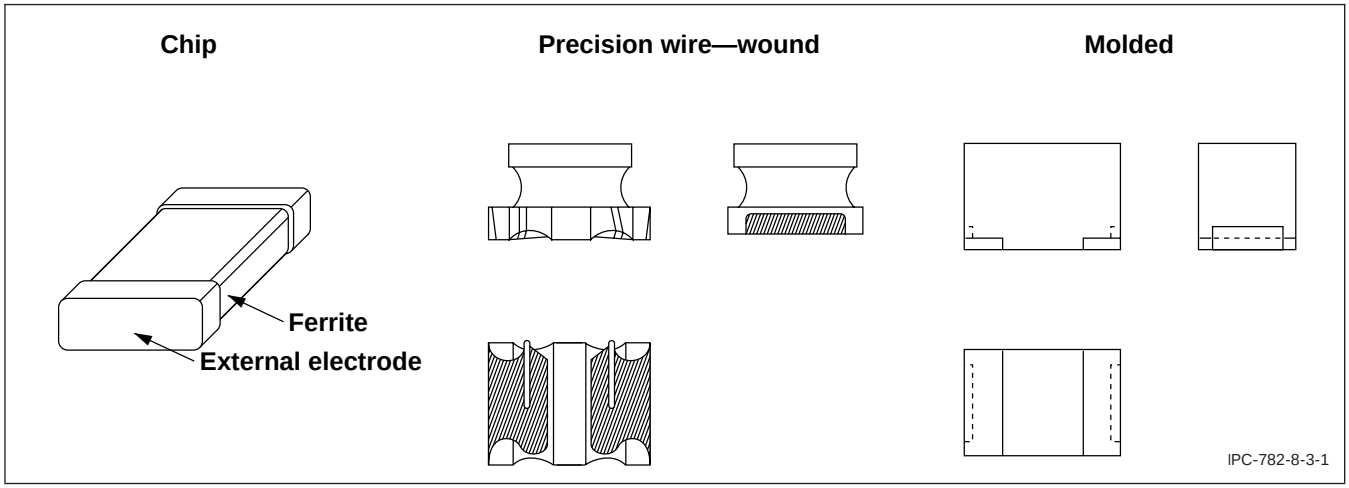
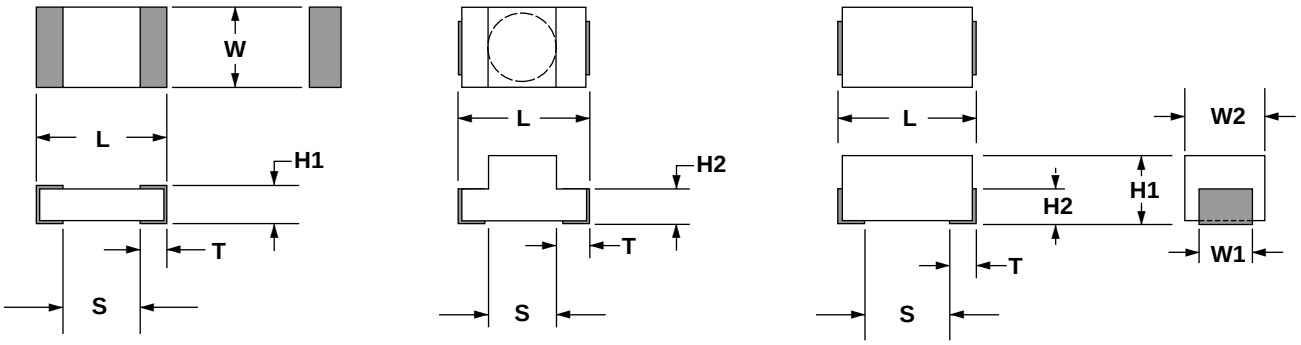


Figure 1 Inductor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for inductors.



Component Identifier (mm)	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H1 (mm)	H2 (mm)
	min	max	min	max	min	max	min	max	min	max	max	max
2012 Chip	1.70	2.30	1.10	1.76	0.60	1.20	—	—	0.10	0.30	1.20	—
3216 Chip	2.90	3.50	1.90	2.63	1.30	1.90	—	—	0.20	0.50	1.90	—
4516 Chip	4.20	4.80	2.60	3.53	0.60	1.20	—	—	0.30	0.80	1.90	—
2825 Prec. w/w	2.20	2.80	0.90	1.62	1.95	2.11	2.10	2.54	0.37	0.65	2.29	0.07
3225 Prec. w/w	2.90	3.50	0.90	1.83	1.40	1.80	—	—	0.50	1.00	2.00	0.50
4532 Prec. w/w	4.20	4.80	2.20	3.13	3.00	3.40	—	—	0.50	1.00	2.80	0.50
5038 Prec. w/w	4.35	4.95	2.81	3.51	2.46	2.62	3.41	3.81	0.51	0.77	3.80	0.76
3225/3230 Molded	3.00	3.40	1.60	2.18	1.80	2.00	2.30	2.70	0.40	0.70	2.40	0.51
4035 Molded	3.81	4.32	0.81	1.60	1.20	1.50	2.92	3.18	1.20	1.50	2.67	1.27
4532 Molded	4.20	4.80	2.30	3.15	2.00	2.20	3.00	3.40	0.65	0.95	3.40	0.50
5650 Molded	5.30	5.50	3.30	4.32	3.80	4.20	4.70	5.30	0.50	1.00	5.80	1.00
8530 Molded	8.25	8.76	5.25	6.04	1.20	1.50	2.92	3.18	1.20	1.50	2.67	1.27

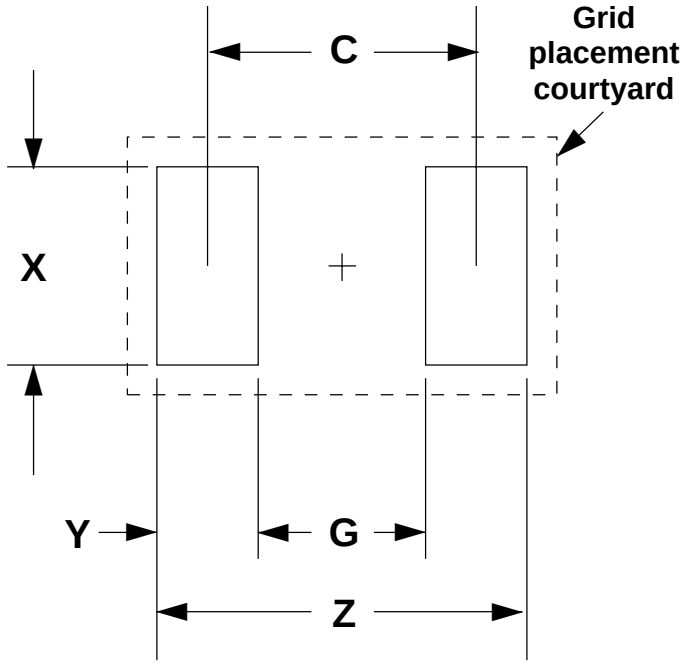
Figure 2 Inductor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for inductors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least mate-rial condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	C (mm) ref	Y (mm) ref	Placement Grid (No. Grid Elements)
160	2012 Chip 0805	3.00	1.00	1.00	2.00	1.00	4x8
161	3216 Chip 1206	4.20	1.80	1.60	3.00	1.20	6x10
162	4516 Chip	5.80	2.60	1.00	4.20	1.60	4x12
163	2825 Prec	3.80	1.00	2.40	2.40	1.40	6x10
164	3225 Prec 1210	4.60	1.00	2.00	2.80	1.80	6x10
165	4532 Prec 1812	5.80	2.20	3.60	4.00	1.80	8x14
166	5038 Prec	5.80	3.00	2.80	4.40	1.40	8x14
167	3225/3230 Molded	4.40	1.20	2.20	2.80	1.60	6x10
168	4035 Molded	5.40	1.00	1.40	3.20	2.20	8x12
169	4532 Molded 1812	5.80	1.80	2.40	3.80	2.00	8x14
170	5650 Molded	6.80	3.20	4.00	5.00	1.80	12x16
171	8530 Molded	9.80	5.00	1.40	7.40	2.40	8x22

Figure 3 Inductor land pattern dimensions

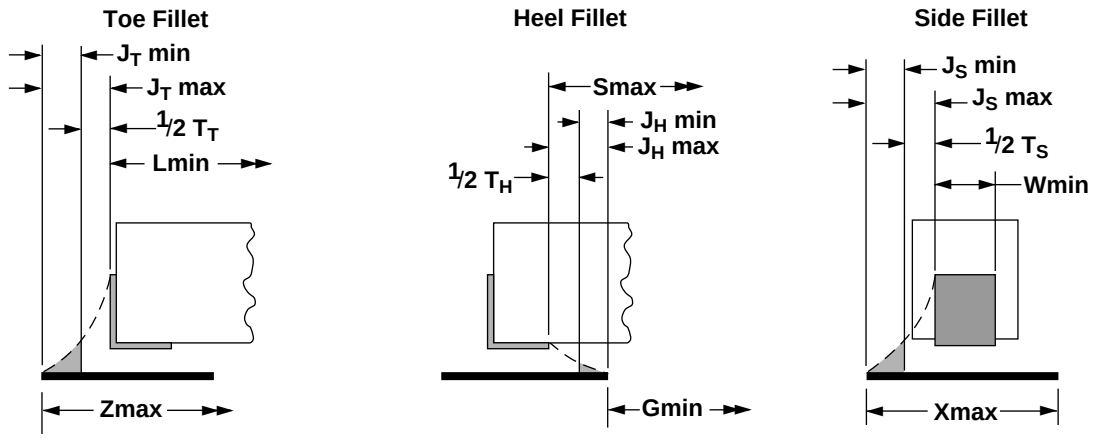
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm) F	P	Solder Joint: Toe (mm) C_L	$J_T$min	$J_T$max	Heel (mm) C_S	$J_H$min	$J_H$max	Side (mm) C_{WI}	$J_S$min	$J_S$max
160	0.2	0.2	0.663	0.32	0.98	0.721	0.02	0.74	0.663	–0.13	0.53
161	0.2	0.2	0.663	0.32	0.98	0.787	0.02	0.81	0.663	–0.18	0.48
162	0.2	0.2	0.663	0.47	1.13	0.970	–0.02	0.95	0.663	–0.13	0.53
163	0.2	0.2	0.663	0.47	1.13	0.773	–0.08	0.70	0.325	0.06	0.39
164	0.2	0.2	0.663	0.52	1.18	0.970	–0.07	0.90	0.490	0.06	0.54
165	0.2	0.2	0.663	0.47	1.13	0.970	–0.02	0.95	0.490	0.05	0.54
166	0.2	0.2	0.663	0.39	1.06	0.758	–0.12	0.64	0.325	0.01	0.33
167	0.2	0.2	0.490	0.46	0.94	0.648	0.17	0.82	0.346	0.03	0.37
168	0.2	0.2	0.583	0.50	1.09	0.837	–0.12	0.72	0.412	–0.11	0.31
169	0.2	0.2	0.663	0.47	1.13	0.894	0.23	1.12	0.346	0.03	0.37
170	0.2	0.2	0.346	0.58	0.92	1.058	0.03	1.09	0.490	–0.14	0.34
171	0.2	0.2	0.583	0.48	1.07	0.837	0.10	0.94	0.412	–0.11	0.31

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as tantalum capacitors.

This subsection provides the component and land pattern dimensions for tantalum capacitors along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the inductor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for tantalum capacitors. The following sections describe the most common types.

3.1 Basic Construction See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Parts are available with or without marked capacitance values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

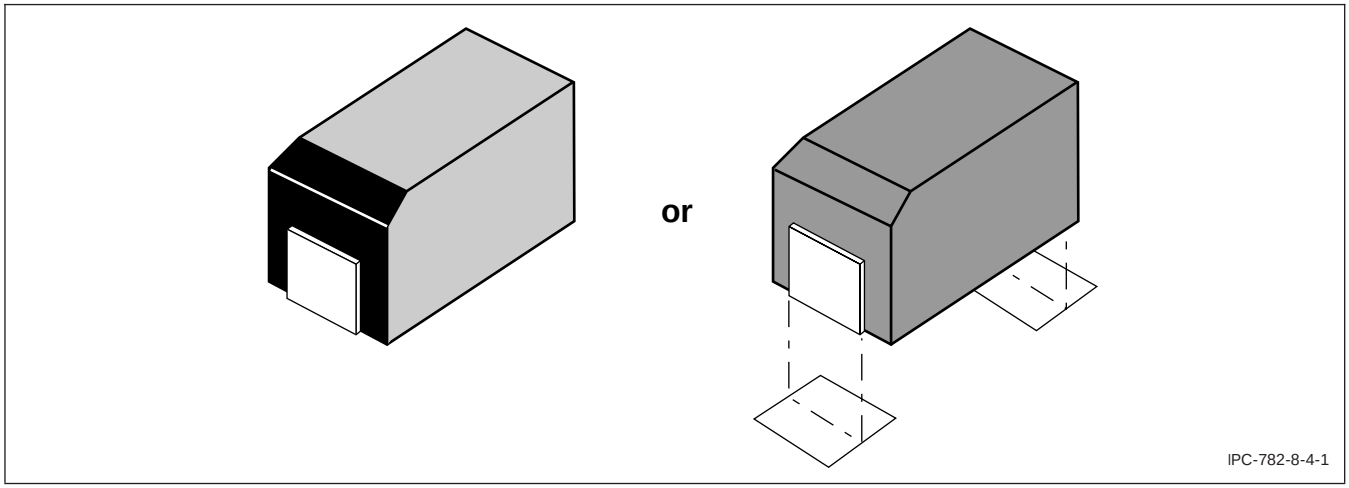
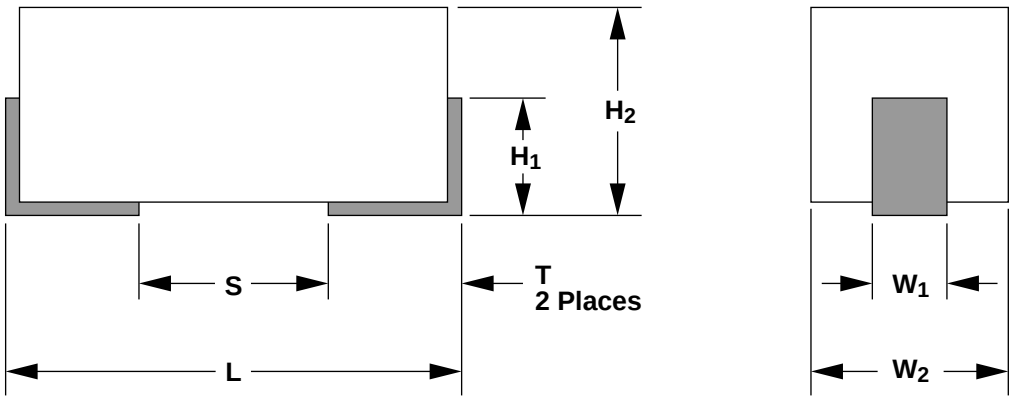


Figure 1 Tantalum capacitor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for tantalum capacitors.



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Component Identifier (mm)	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H1 (mm)	H2 (mm)
	min	max	min	max	min	max	min	max	min	max	min	max
3216	3.00	3.40	0.80	1.74	1.17	1.21	1.40	1.80	0.50	1.10	0.70	1.80
3528	3.30	3.70	1.10	2.04	2.19	2.21	2.60	3.00	0.50	1.10	0.70	2.10
6032	5.70	6.30	2.50	3.54	2.19	2.21	2.90	3.50	1.00	1.60	1.00	2.80
7343	7.00	7.60	3.80	4.84	2.39	2.41	4.00	4.60	1.00	1.60	1.00	3.10

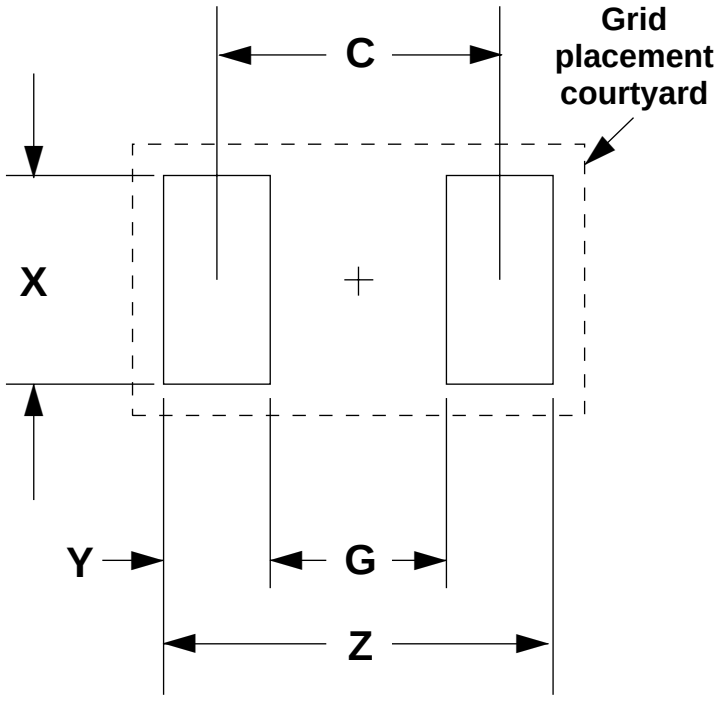
Figure 2 Tantalum capacitor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for tantalum capacitors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
180A	3216	4.80	0.80	1.20	2.00	2.80	6x12
181A	3528	5.00	1.00	2.20	2.00	3.00	8x12
182A	6032	7.60	2.40	2.20	2.60	5.00	8x18
183A	7343	9.00	3.80	2.40	2.60	6.40	10x20

Figure 3 Tantalum capacitor land pattern dimensions

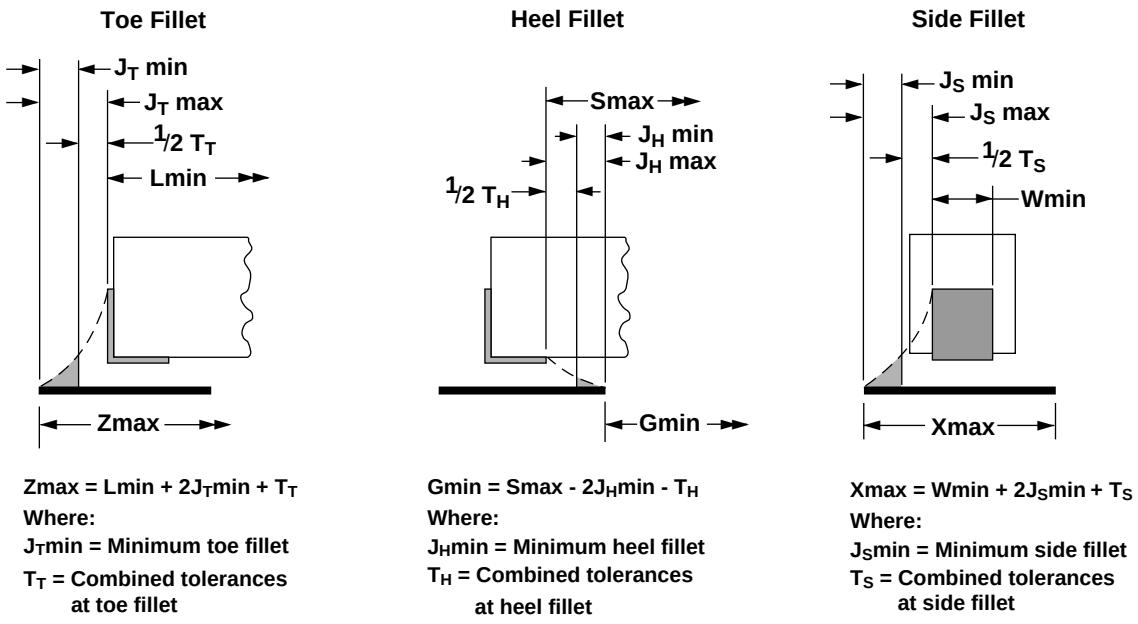
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2$J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - 2$J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + 2$J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
180A	0.10	0.10	0.40	0.69	1.11	0.94	–0.01	0.94	0.40	–0.20	0.23
181A	0.10	0.10	0.40	0.64	1.06	0.94	0.04	0.99	0.40	–0.21	0.22
182A	0.10	0.10	0.60	0.64	1.26	1.04	0.05	1.09	0.60	–0.30	0.31
183A	0.10	0.10	0.60	0.69	1.31	1.04	–0.00	1.04	0.60	–0.30	0.31

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for metal electrode face components (MELFs). Basic construction of the MELF device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

Resistors, ceramic capacitors, and tantalum capacitors may all be packaged in these tubular shapes.

3.1 Basic Construction See Figures 1a and 1b.

3.1.1 Termination Materials End terminations should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick. The terminations should be symmetrical, and should not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part.

The most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick. The end termination shall cover the ends of the components, and shall extend around the entire periphery.

3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

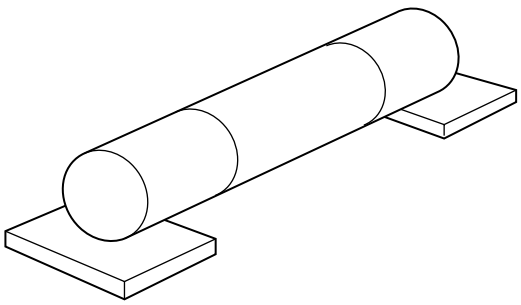

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Figure 1a Metal electrode face component construction

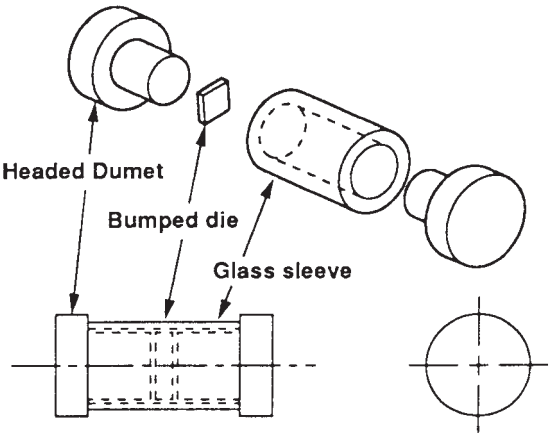

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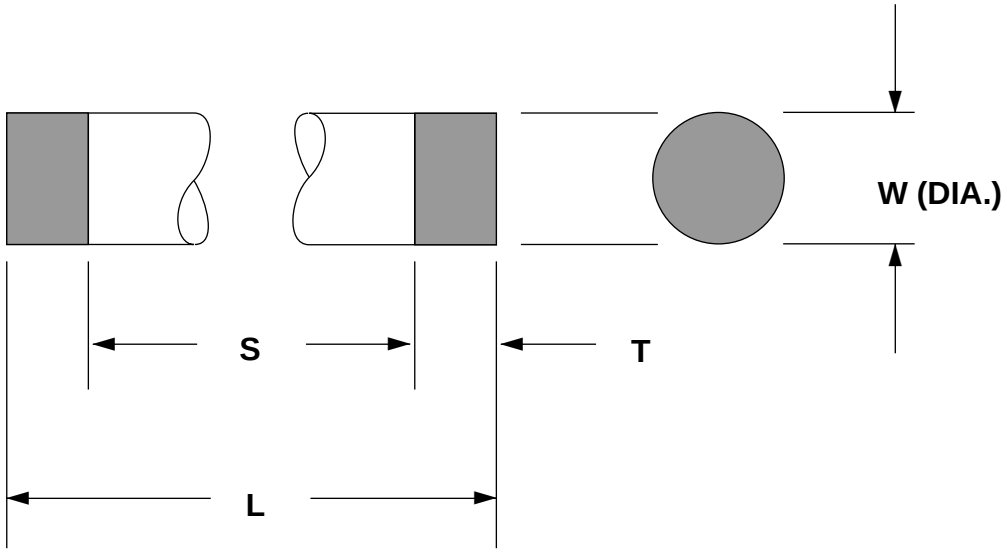
Figure 1b Break-away diagram of MELF components

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for metal electrode face components (MELFs).



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Component Identifier (mm) [in]	L (mm)		S (mm)		W (mm)		T (mm)		Component Type
	min	max	min	max	min	max	min	max	
SOD-80/MLL 34	3.30	3.70	2.20	2.65	1.60	1.70	0.41	0.55	Diode
SOD-87/MLL 41	4.80	5.20	3.80	4.25	2.44	2.54	0.36	0.50	Diode
2012 [0805]	1.90	2.10	1.16	1.44	1.35	1.45	0.23	0.37	0.10 mW resistor
3216 [1206]	3.00	3.40	1.86	2.31	1.75	1.85	0.43	0.57	0.25 mW resistor
3516 [1406]	3.30	3.70	2.16	2.61	1.55	1.65	0.43	0.57	0.12 W resistor
5923 [2309]	5.70	6.10	4.36	4.81	2.40	2.50	0.53	0.67	0.25 W resistor

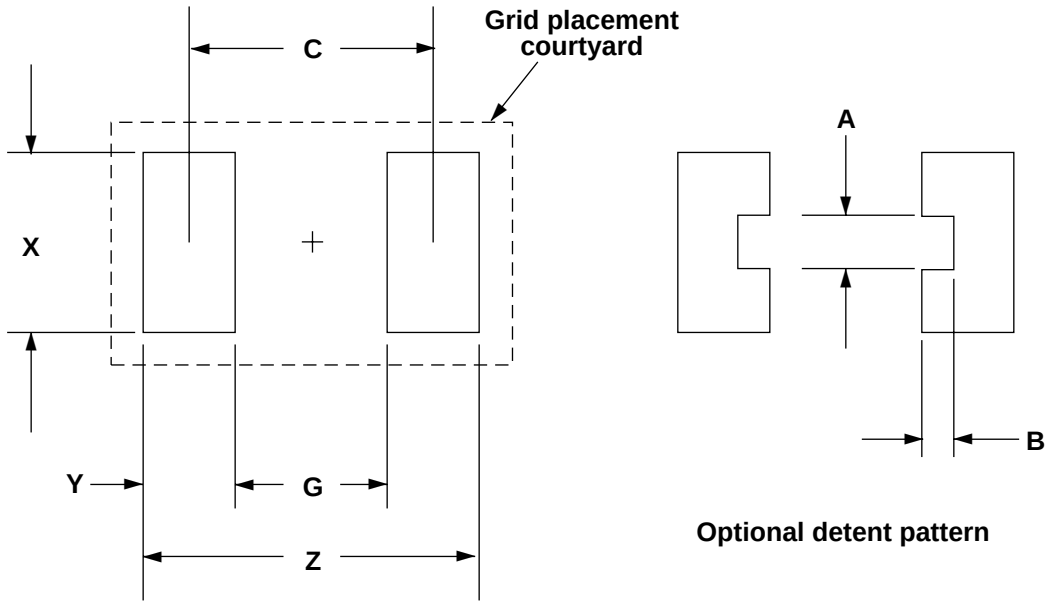
Figure 2 Metal electrode face component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for metal electrode face components (MELFs). These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm) [in]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	A	B	Placement Grid (No. of Grid Elements)
200A	SOD-80/MLL-34	4.80	2.00	1.80	1.40	3.40	0.50	0.50	6x12
201A	SOD-87/MLL-41	6.30	3.40	2.60	1.45	4.85	0.50	0.50	6x14
202A	2012 [0805]	3.20	0.60	1.60	1.30	1.90	0.50	0.35	4x8
203A	3216 [1206]	4.40	1.20	2.00	1.60	2.80	0.50	0.55	6x10
204A	3516 [1406]	4.80	2.00	1.80	1.40	3.40	0.50	0.55	6x12
205A	5923 [2309]	7.20	4.20	2.60	1.50	5.70	0.50	0.65	6x18

Figure 3 Metal electrode face component land pattern dimensions

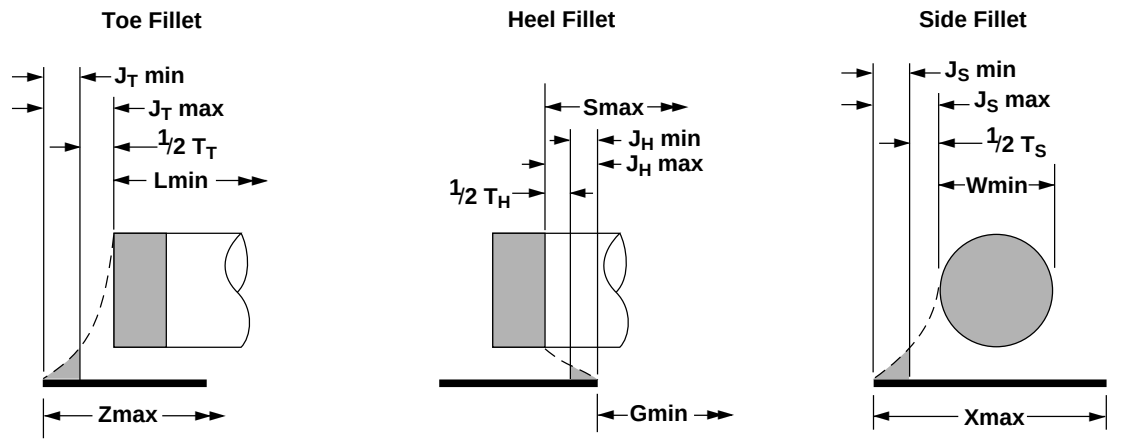
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2$J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - 2$J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + 2$J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
200A	0.10	0.10	0.40	0.54	0.96	0.45	0.09	0.56	0.10	0.01	0.19
201A	0.10	0.10	0.40	0.54	0.96	0.45	0.19	0.66	0.10	-0.01	0.17
202A	0.10	0.10	0.20	0.53	0.77	0.28	0.26	0.58	0.10	0.04	0.21
203A	0.10	0.10	0.40	0.49	0.91	0.45	0.32	0.79	0.10	0.04	0.21
204A	0.10	0.10	0.40	0.54	0.96	0.45	0.07	0.54	0.10	0.04	0.21
205A	0.10	0.10	0.40	0.54	0.96	0.45	0.07	0.54	0.10	0.01	0.19

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 23 (small outline transistor) components. Basic construction of the SOT 23 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

One of the first active devices in packaged form for surface mounting was the SOT device. Plastic encapsulated three terminal devices with leads formed out from the body were surface mounted to overcome some of the problems and difficulties in handling dip transistors. In general, SOT packages are used with diodes, transistors, and small I/O devices.

The SOT 23 package is the most common three-lead surface mount configuration.

3.1 Basic Construction The SOT 23 package has had several redesigns to meet the needs of both hybrid and printed board surface mount industries. These changes resulted in low, medium and high profile characteristics which basically reflect the clearance that the body is from the mounting surface. See Figure 1 for construction characteristics and Figure 2 for dimensions.

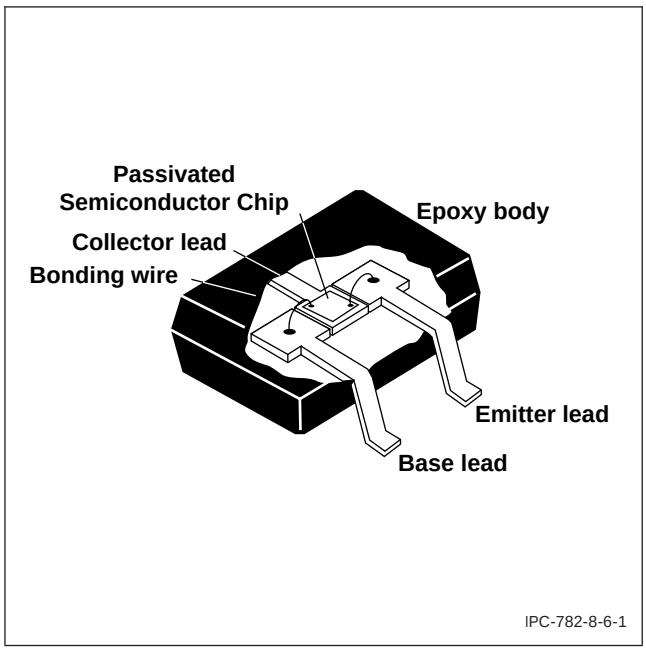


Figure 1 SOT 23 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

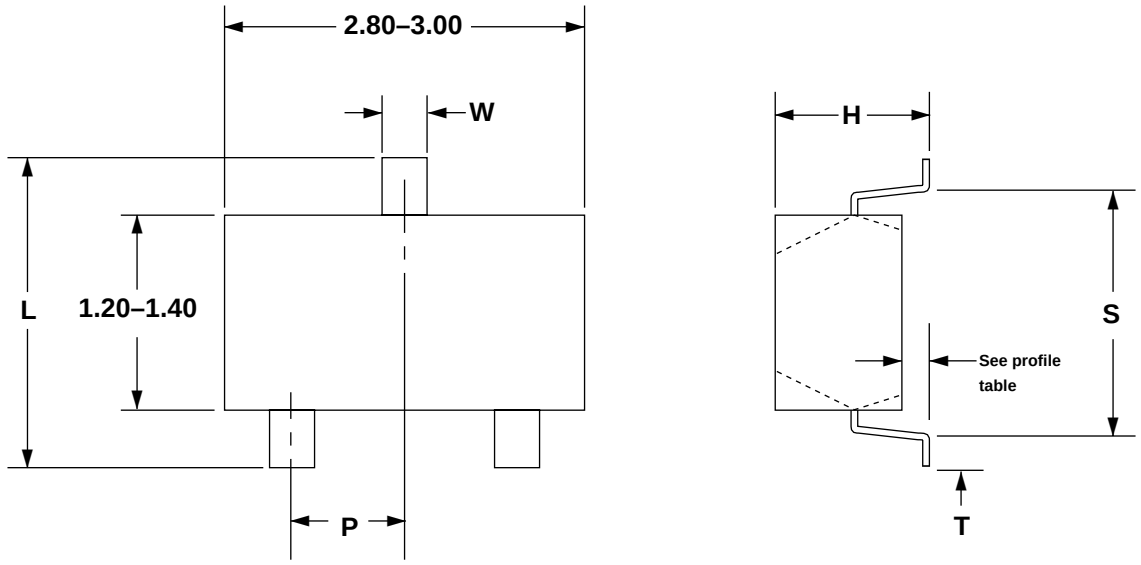
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-236, 8 mm tape/4 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 23 components.



Profile	Dimension	TO 236 Des
Low	0.01–0.10	AB
Medium	0.08–0.13	——
High	0.1–0.25	AA

Dimensions are in millimeters

IPC-782-8-6-2

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	max	nom
SOT 23	2.30	2.60	1.10	1.47	0.36	0.46	0.45	0.60	1.10	0.95

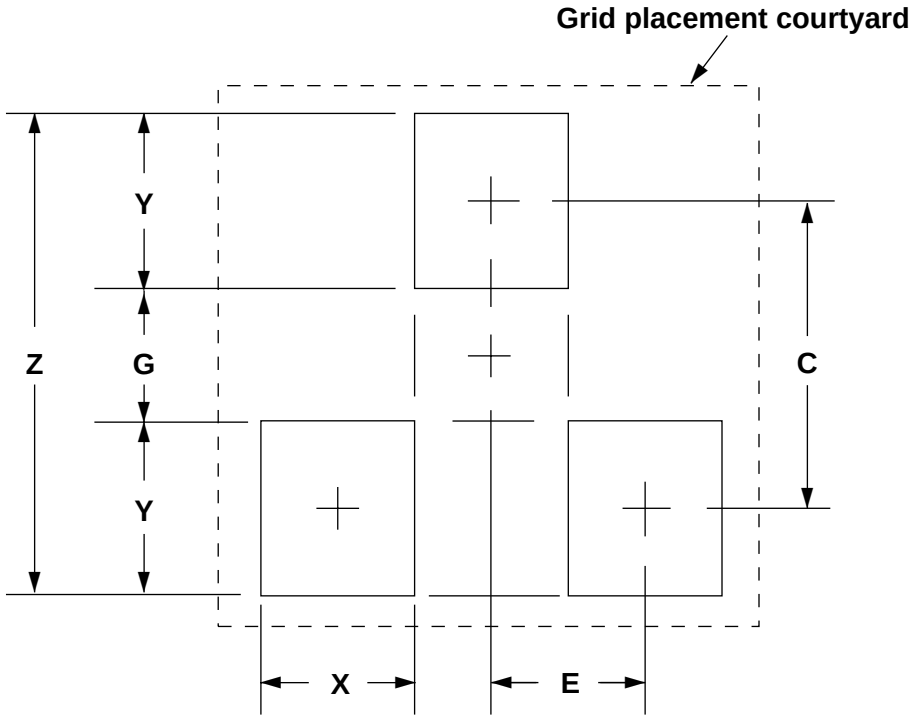
Figure 2 SOT 23 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 23 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
210	SOT 23 (reflow solder)	3.60	0.80	1.00	1.40	2.20	0.95	8x8

*Note: If a more robust pattern is desired for wave soldering, add 0.2 mm to "Z" and identify as RLP 210W.

Figure 3 SOT 23 land pattern dimensions

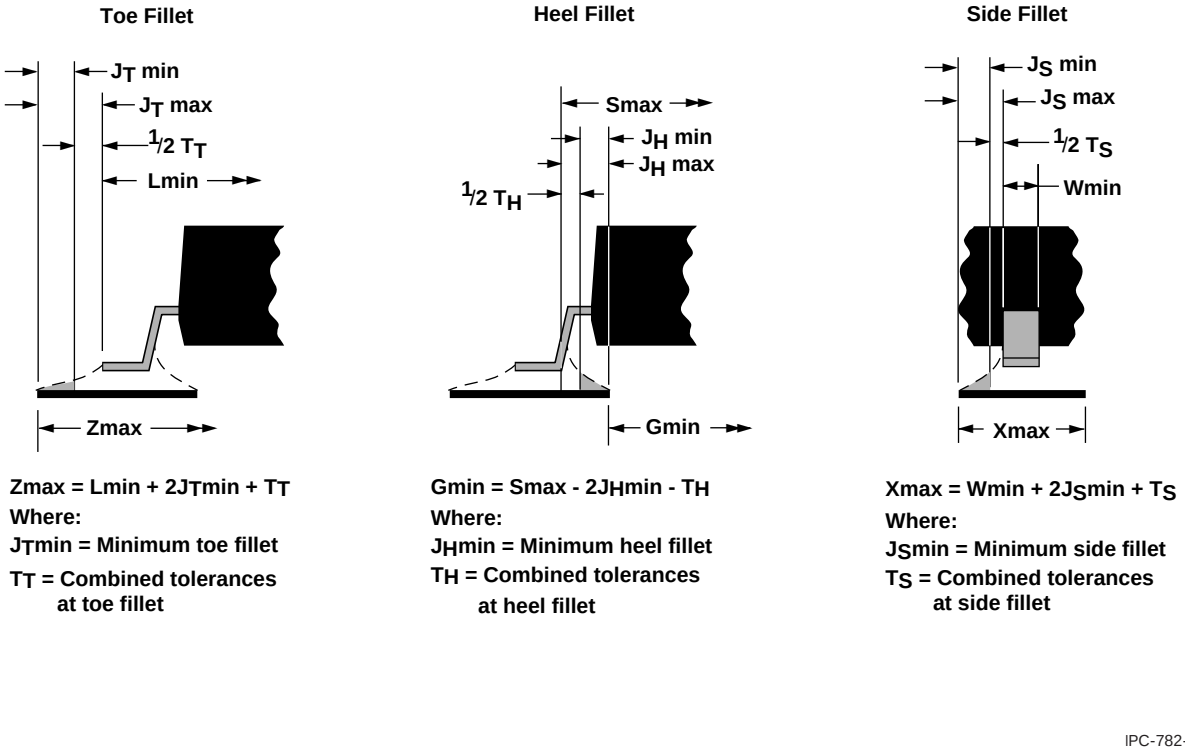
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2JTmin + TT
Where:
JTmin = Minimum toe fillet
TT = Combined tolerances at toe fillet

Gmin = Smax - 2JHmin - TH
Where:
JHmin = Minimum heel fillet
TH = Combined tolerances at heel fillet

Xmax = Wmin + 2JSmin + TS
Where:
JSmin = Minimum side fillet
TS = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
210	0.2	0.2	0.30	0.44	0.65	0.37	0.10	0.33	0.10	0.17	0.32

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**8.7**
Revision	Subject
	SOT 89

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 89 (small outline transistor) components. Basic construction of the SOT 89 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Pubication 95 Registered and Standard Outlines for Solid State and Related Products, TO-243, Issue ''C'' dated 7/15/86

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for high power transistors and diodes. These parts are used where heat transfer to a supporting structure is important.

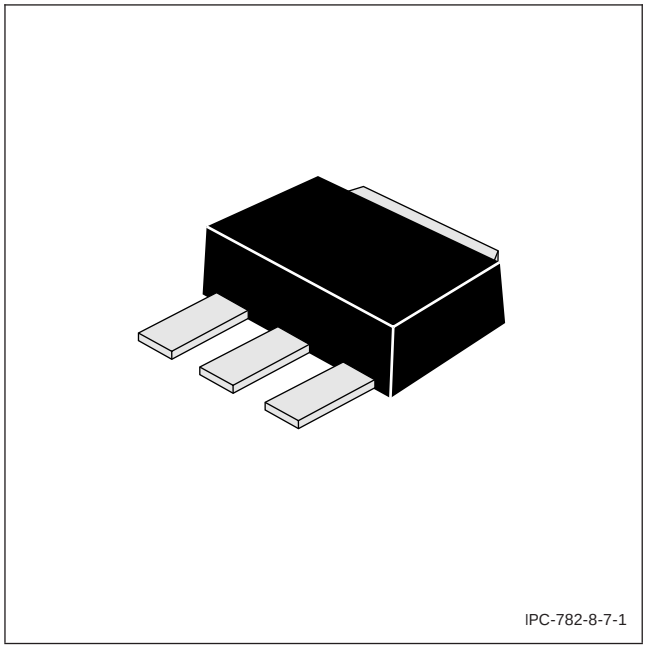


Figure 1 SOT 89 construction

3.1 Basic Construction See Figure 1. The SOT 89 package dimensions are designed to meet the needs of both the hybrid and printed board surface mount industries. In order to provide an adequate heat transfer path, there is no clearance between the body of the component and the packaging and interconnect structure. This design may accommodate the reflow or wave soldering processes.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

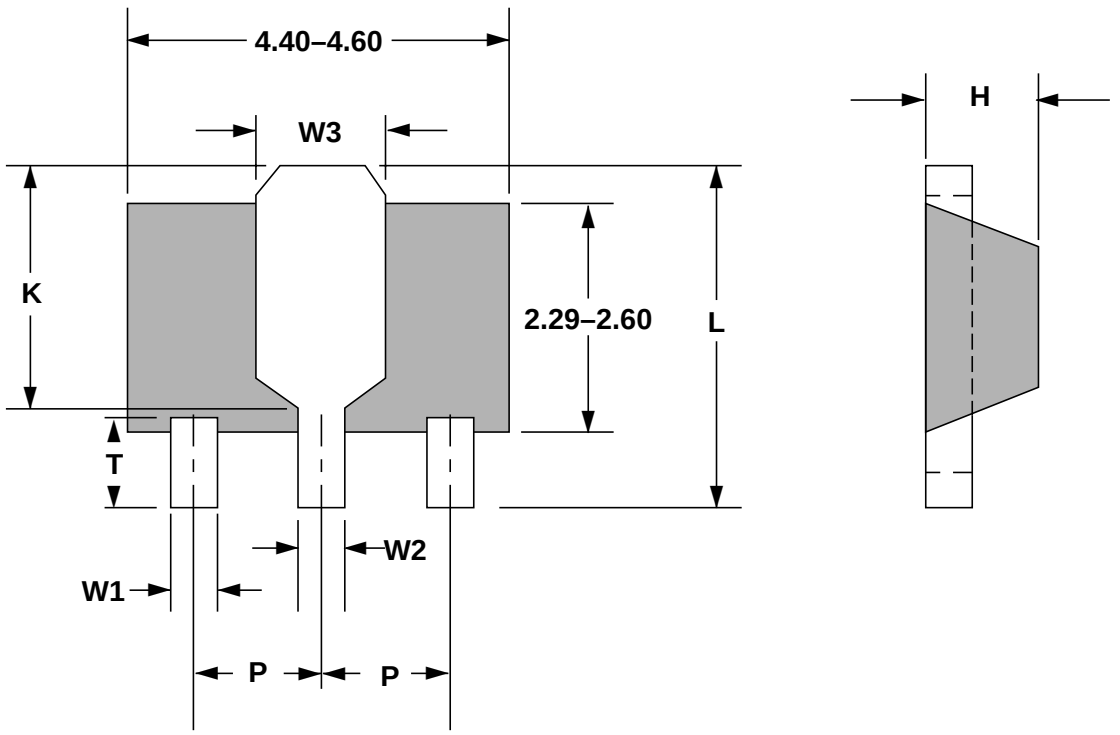
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-243, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 89 components.



Dimensions are in millimeters.

IPC-782-8-7-2

Component Identifier	L (mm)		T (mm)		W1 (mm)		W2 (mm)		W3 (mm)		K (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	max	basic
SOT 89	3.94	4.25	0.89	1.20	0.36	0.48	0.44	0.56	1.62	1.83	2.60	2.85	1.60	1.50

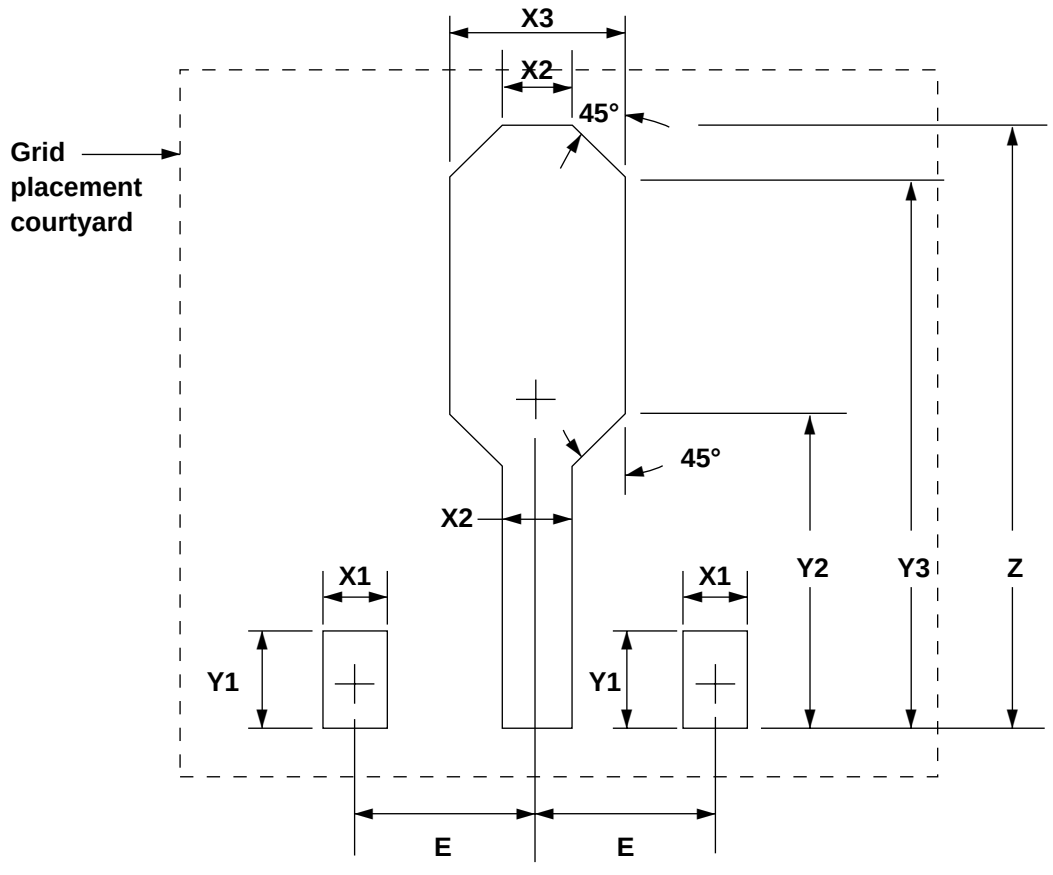
Figure 2 SOT 89 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 89 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	Y1 (mm)	X1 (mm)	X2 (mm)		X3 (mm)		Y2 (mm)	Y3 (mm)	E (mm)	Placement Grid (No. of Grid Elements)
					min	max	min	max	ref	ref	basic	
215	SOT 89	5.40	1.40	0.80	0.80	1.00	1.80	2.00	2.40	4.60	1.50	12x10

Figure 3 SOT 89 land pattern dimensions

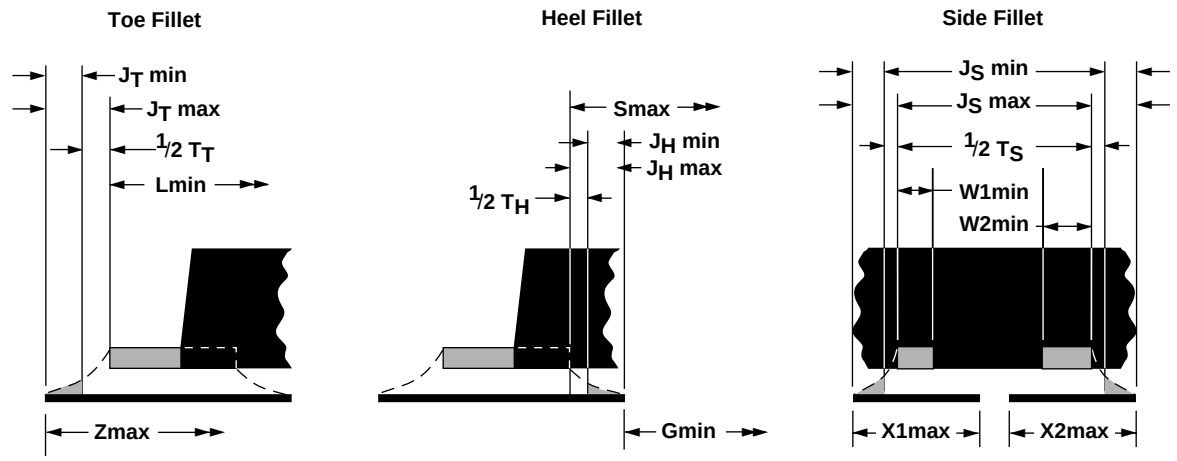
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2JTmin + TT
Where:
JTmin = Minimum toe fillet
TT = Combined tolerances at toe fillet

Gmin = Smax - 2JHmin - TH
Where:
JHmin = Minimum heel fillet
TH = Combined tolerances at heel fillet

Xmax = Wmin + 2JSmin + TS
Where:
JSmin = Minimum side fillet
TS = Combined tolerances at side fillet

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RLP No.	Tolerance Assumptions (mm)		Solder Joint														
			Toe (mm)			Heel (mm)			Side (X1) (mm)			Side (X2) (mm)			Side (X3) (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max	C_{W3}	J_{S3}min	J_{S3}max
215	0.2	0.2	0.31	0.52	0.68	0.31	0.15	0.30	0.12	0.07	0.13	0.12	0.13	0.19	0.21	0.01	0.12

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**8.8**
Revision	Subject
A	**SOD 123**

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOD 123 (small outline diode) components. Basic construction of the SOD 123 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, DO-214, Issue ''B'' dated 3/91

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

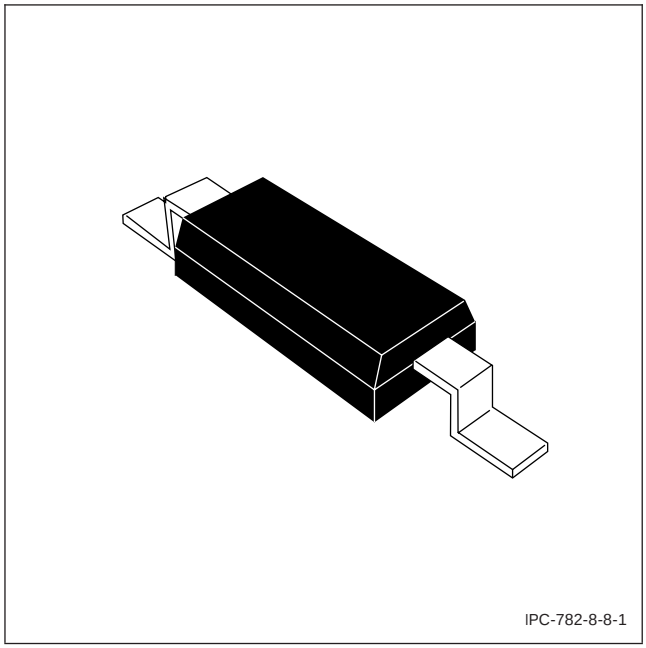


Figure 1 SOD 123 construction

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction The small outline diode comes in two configurations. One is gullwing-leaded as shown in Figure 1. The other is molded with terminations as dimensioned in Figure 2.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

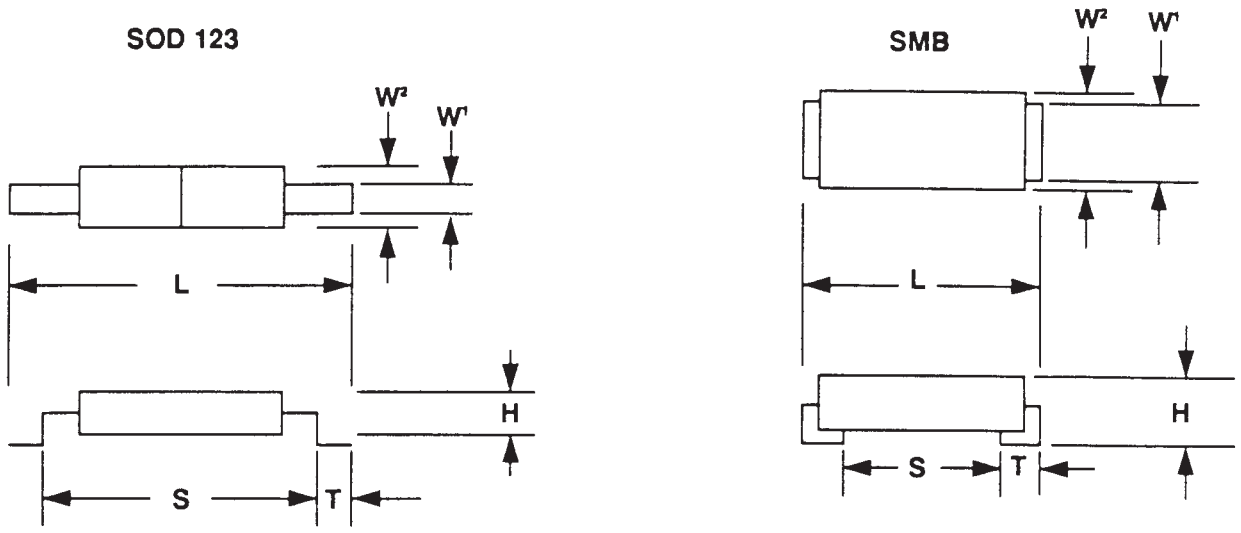
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package formats are tape and reel; 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOD 123 components.



IPC-782-8-8-2

Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H
	min	max	min	max	min	max	min	max	min	max	max
SOD 123	3.55	3.85	2.35	2.93	0.45	0.65	1.40	1.70	0.25	0.60	1.35
SMB	5.21	5.59	2.17	3.31	1.96	2.21	3.30	3.94	0.76	1.52	2.41

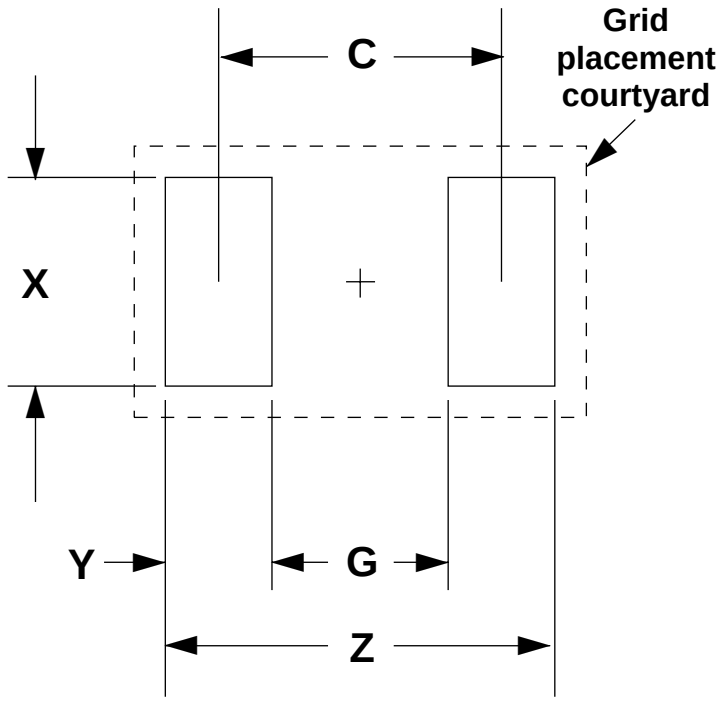
Figure 2 SOD 123 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOD 123 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	X-Z Placement Grid (No. of Grid Elements)
220A	SOD 123	5.00	1.80	0.80	1.60	3.40	4X12
221A	SMB	6.80	2.00	2.40	2.40	4.40	8X16

Figure 3 SOD 123 land pattern dimensions

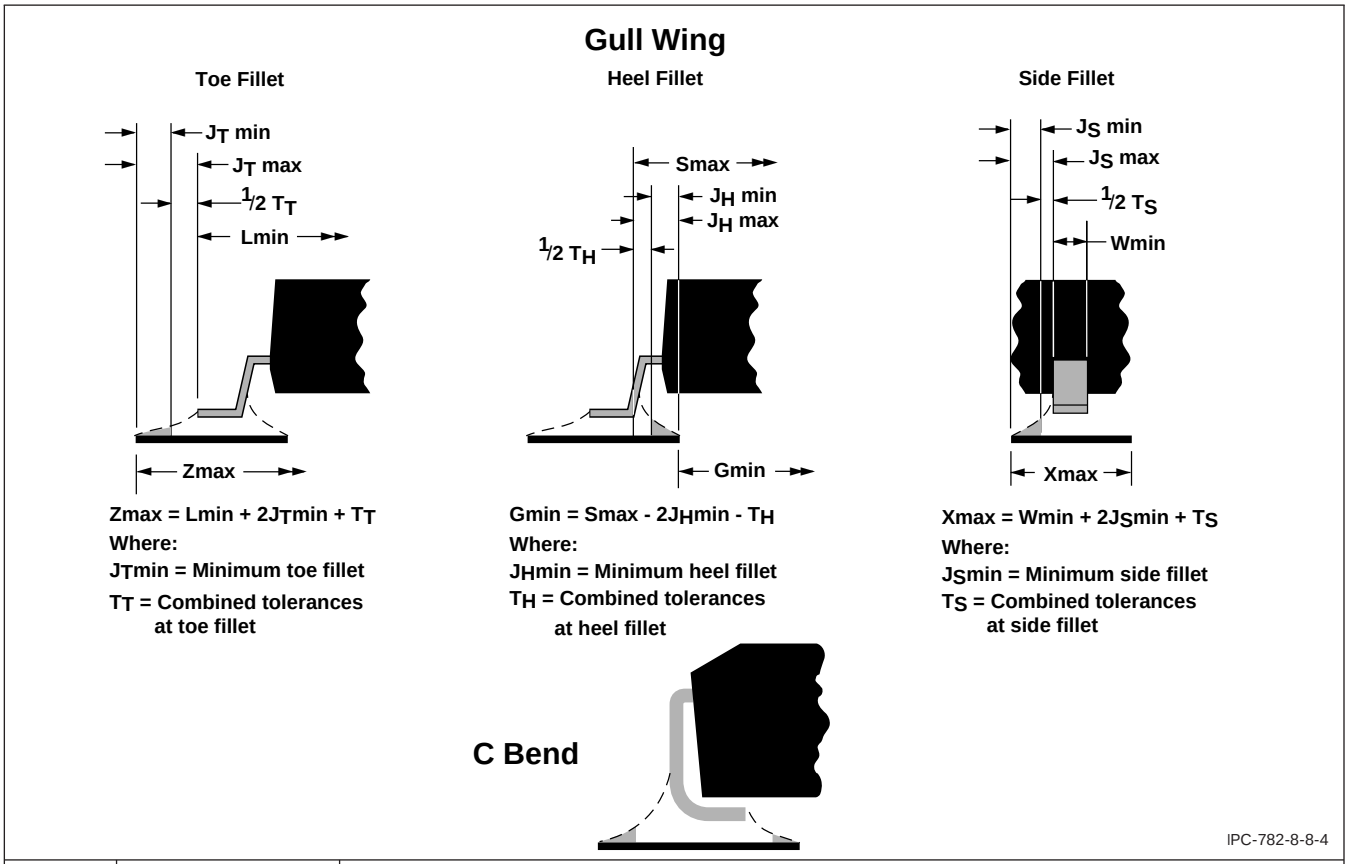
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	$J_S$min	$J_S$max
220A	0.2	0.2	0.30	0.52	0.93	0.58	0.24	0.89	0.20	0.00	0.35
221A	0.2	0.2	0.38	0.56	1.03	0.82	0.07	1.24	0.15	0.03	0.41

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 143 (small outline transistor) components. Basic construction of the SOT 143 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-253, Issue ''C'' dated 11/14/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1. The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.05 to 0.13 mm [0.002 to 0.005 in] to accommodate reflow or wave soldering processes.

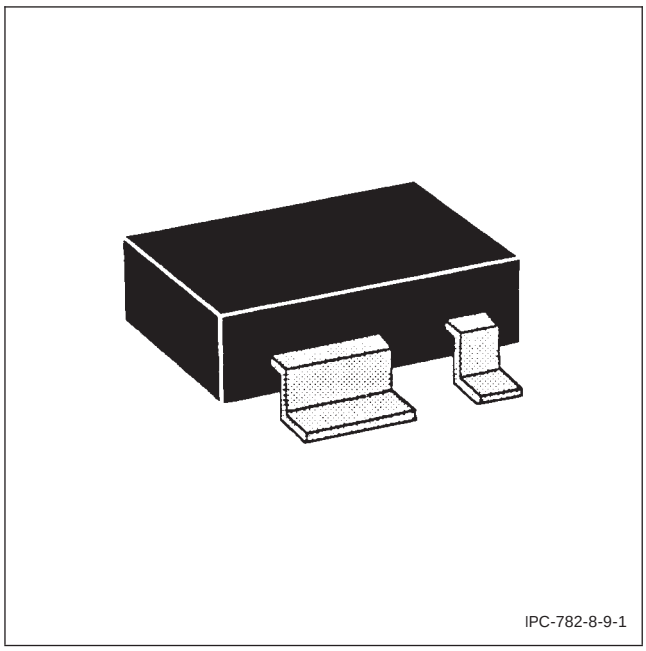


Figure 1 SOT 143 construction

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

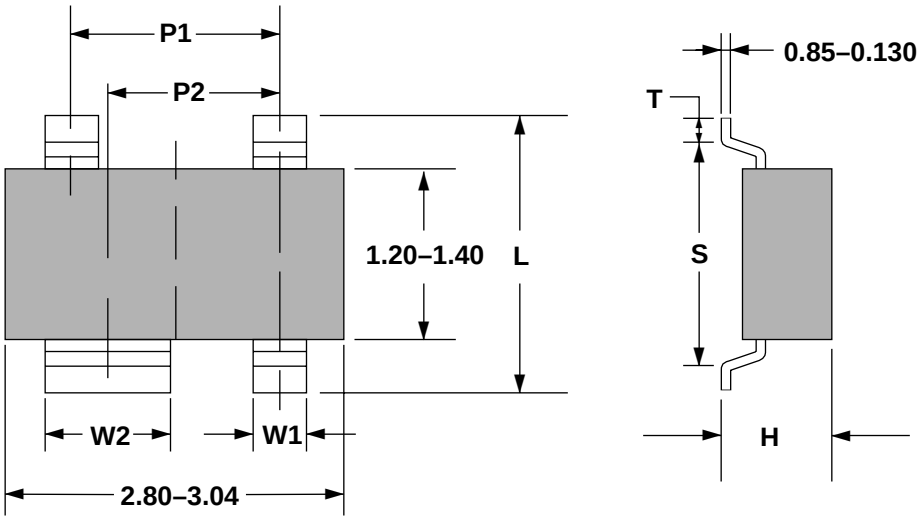
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-253, 8 mm tape/4 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 143 components.



IPC-782-8-9-2

Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		P1 (mm)	P2 (mm)	H (mm)
	min	max	min	max	min	max	min	max	min	max	basic	basic	max
SOT 143	2.10	2.64	1.00	1.69	0.37	0.46	0.76	0.89	0.25	0.55	1.92	1.72	1.20

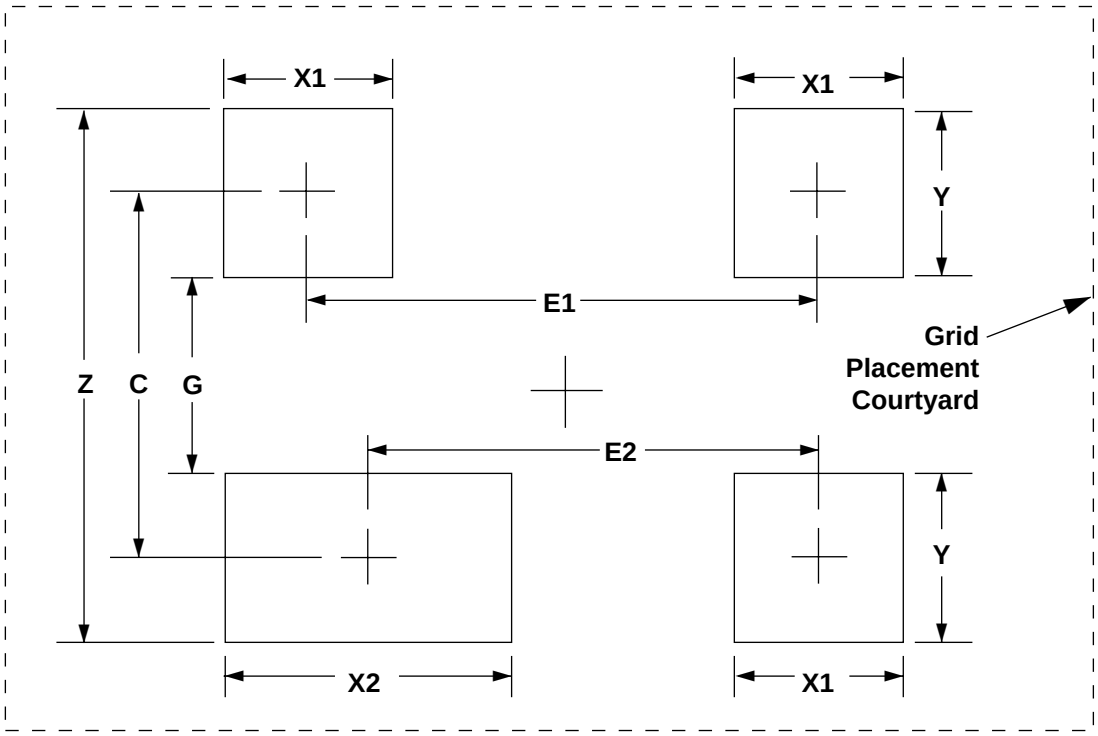
Figure 2 SOT 143 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 143 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



IPC-782-8-9-3

RLP No.	Component Identifier	Z (mm)	G (mm)	X1 (mm)	X2 (mm) min	X2 (mm) max	C ref	E1 Basic	E2 Basic	Y ref	Placement Grid (No. of Grid elements)
225	SOT 143	3.60	0.80	1.00	1.00	1.20	2.20	1.90	1.70	1.40	8x8

Figure 3 SOT 143 land pattern dimensions

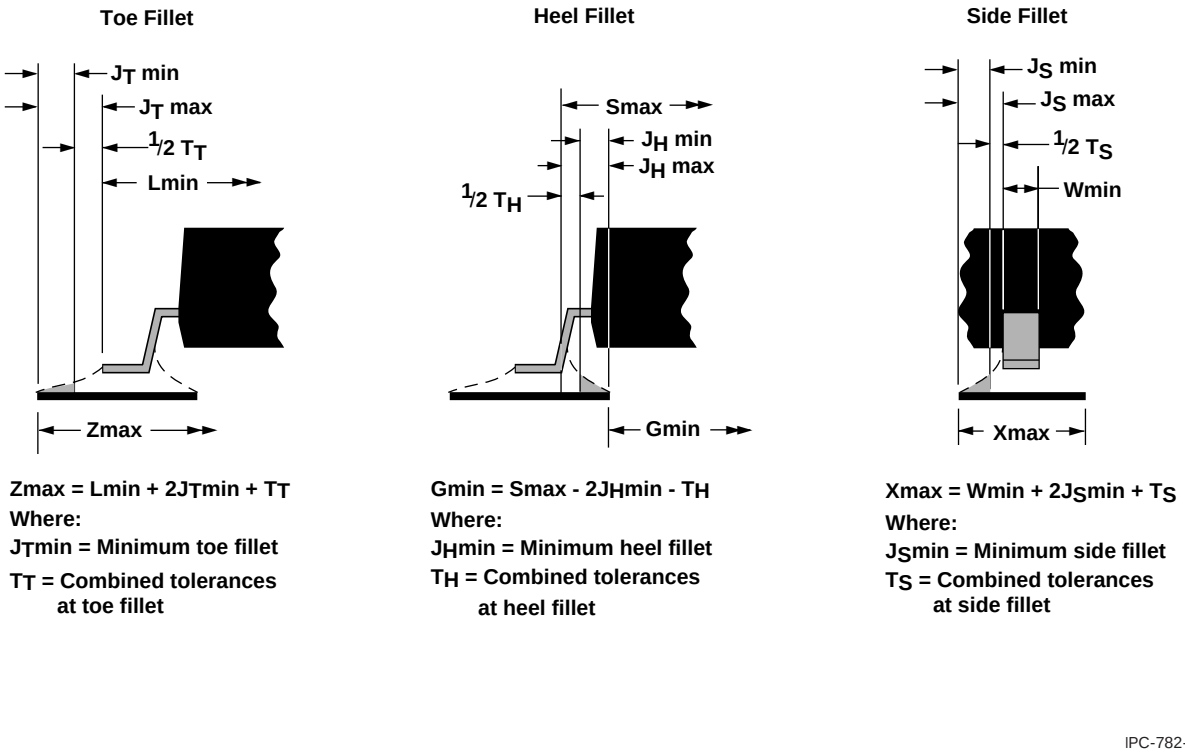
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2JTmin + TT
Where:
JTmin = Minimum toe fillet
TT = Combined tolerances at toe fillet

Gmin = Smax - 2JHmin - TH
Where:
JHmin = Minimum heel fillet
TH = Combined tolerances at heel fillet

Xmax = Wmin + 2JSmin + TS
Where:
JSmin = Minimum side fillet
TS = Combined tolerances at side fillet

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RLP No.	Tolerance Assumptions (mm)		Solder Joint											
			Toe (mm)			Heel (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max
225	0.20	0.20	0.40	0.44	0.75	0.58	0.07	0.44	0.09	0.17	0.31	0.13	0.19	0.37

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 223 (small outline transistor) components. Basic construction of the SOT 223 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-261, Issue ''C'' dated 1/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1. The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.06 mm (basic) to accommodate reflow or wave soldering processes.

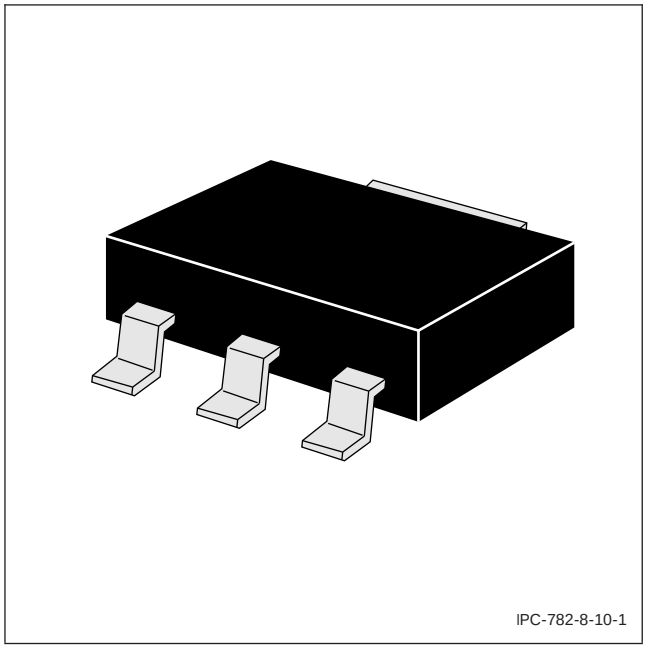


Figure 1 SOT 223 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

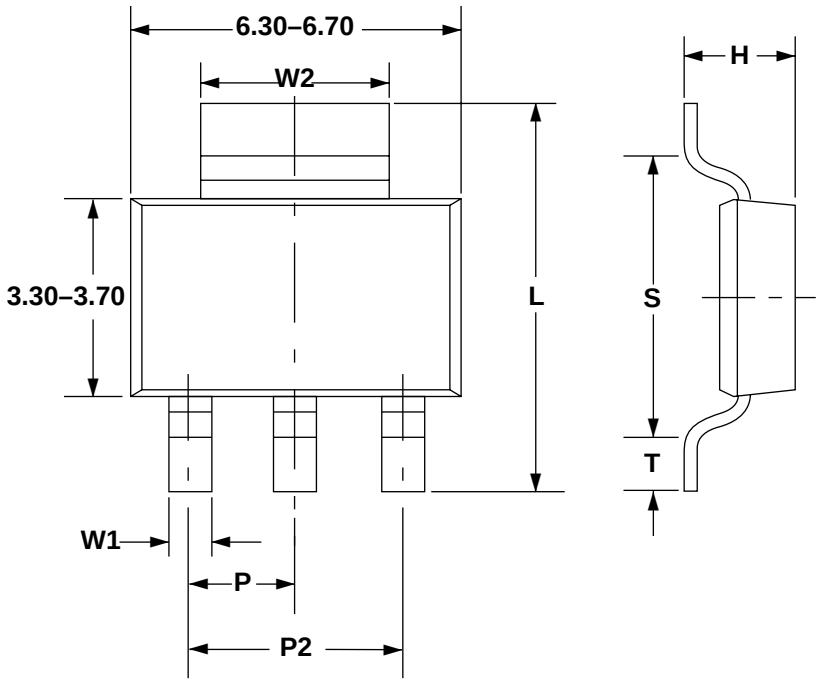
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-261, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 223 components.



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Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H	P1	P2
	min	max	min	max	min	max	min	max	min	max	max	basic	basic
SOT 223	6.70	7.30	4.10	4.92	0.60	0.88	2.90	3.18	0.90	1.30	1.80	2.30	4.60

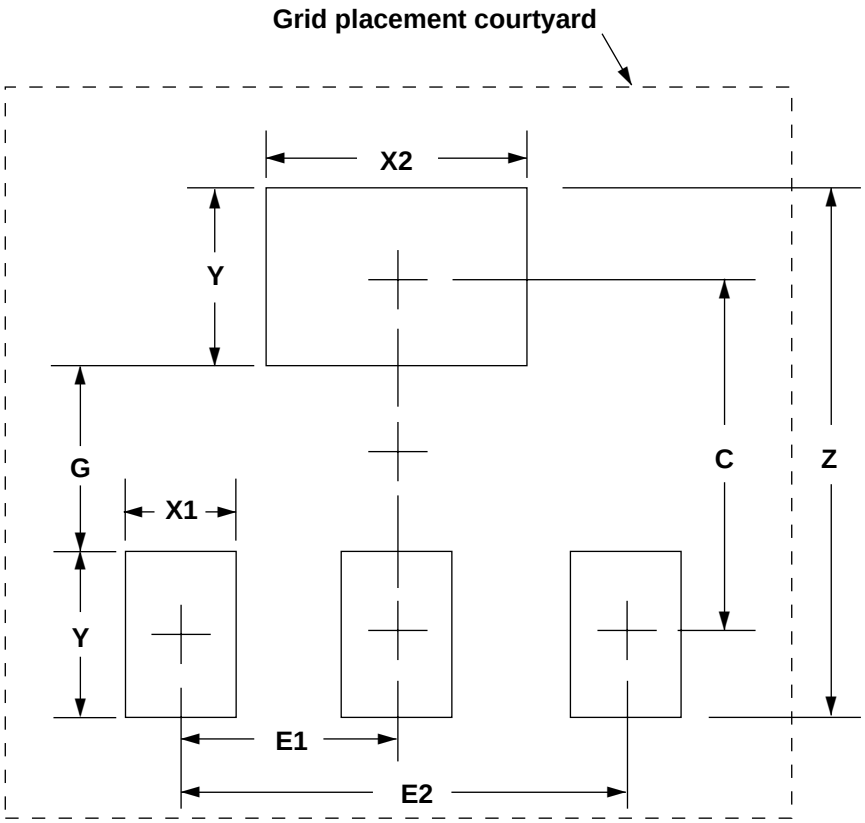
Figure 2 SOT 223 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 223 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X1 (mm)	X2 (mm)		Y (mm)	C (mm)	E1 (mm)	E2 (mm)	Placement Grid (No. of Grid Elements)
					min	max	ref	ref	basic	basic	
230	SOT 223	8.40	4.00	1.20	3.40	3.60	2.20	6.20	2.30	4.60	18x14

Figure 3 SOT 223 land pattern dimensions

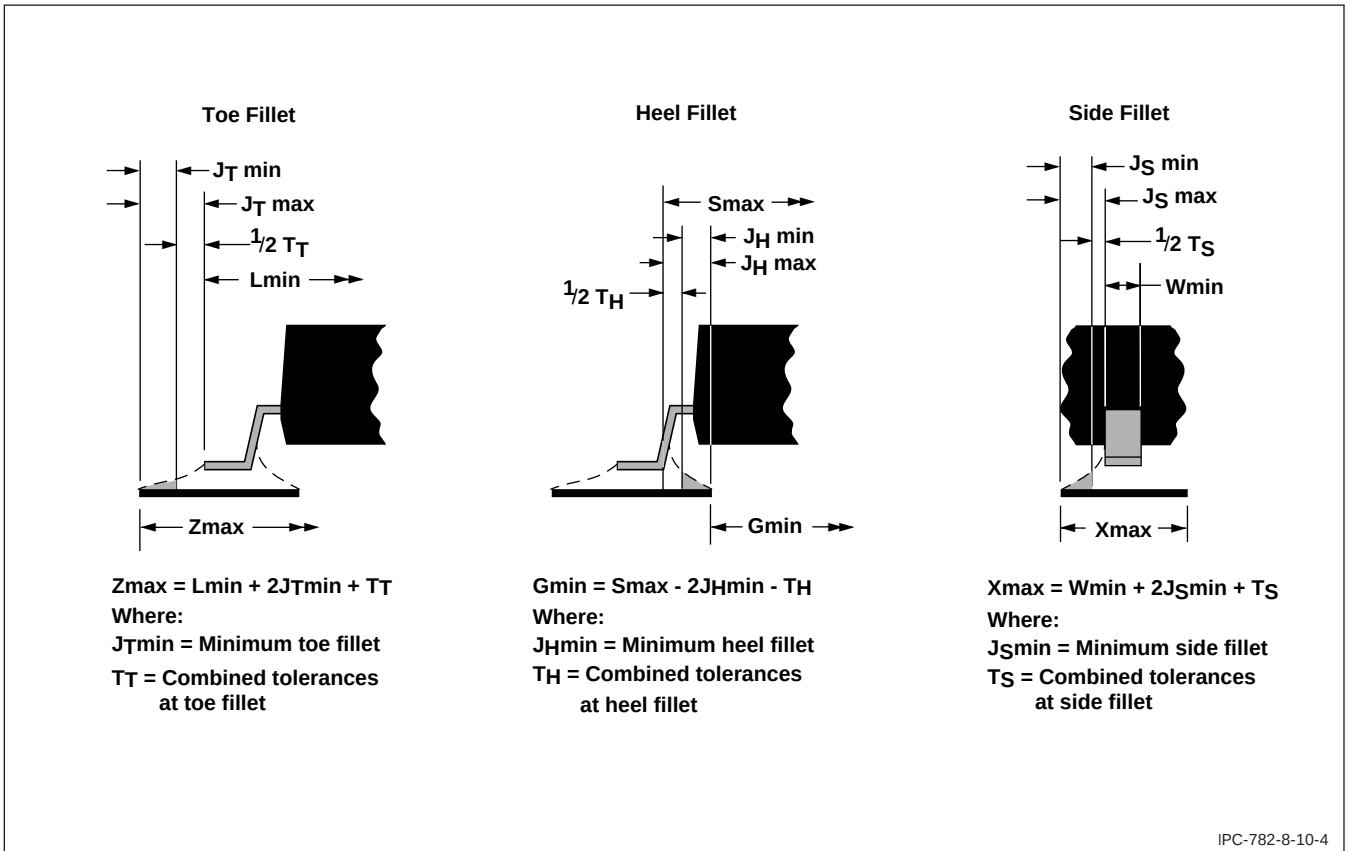
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint											
			Toe (mm)			Heel (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$H_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max
230	0.2	0.2	0.60	0.52	0.85	0.825	0.03	0.46	0.20	0.10	0.30	0.20	0.13	0.35

Figure 4 Tolerance and solder joint analysis

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Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**8.11**
Revision	Subject
A	**TO 252/TO 268**

1.0 SCOPE

This subsection provides the component and land pattern dimensions for TO 252 (small outline transistor) components. Basic construction of the TO 252 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-252, Issue ''B'' dated 9/88

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1.

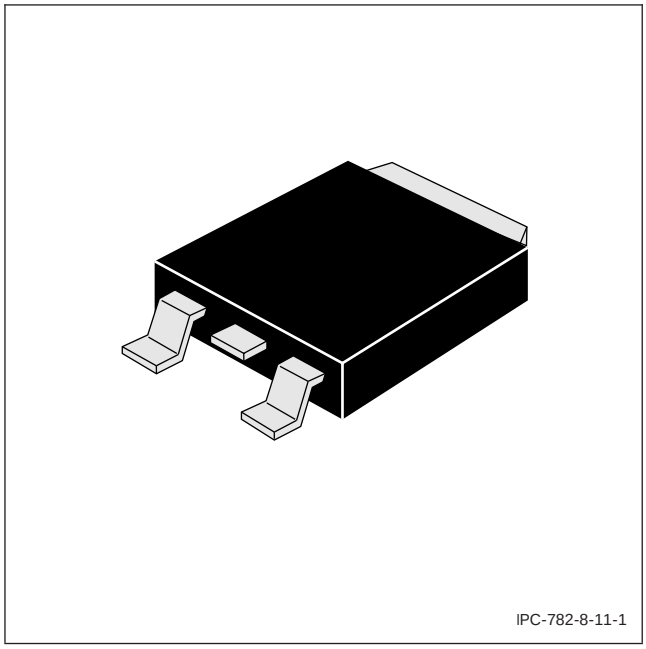


Figure 1 TO 252 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

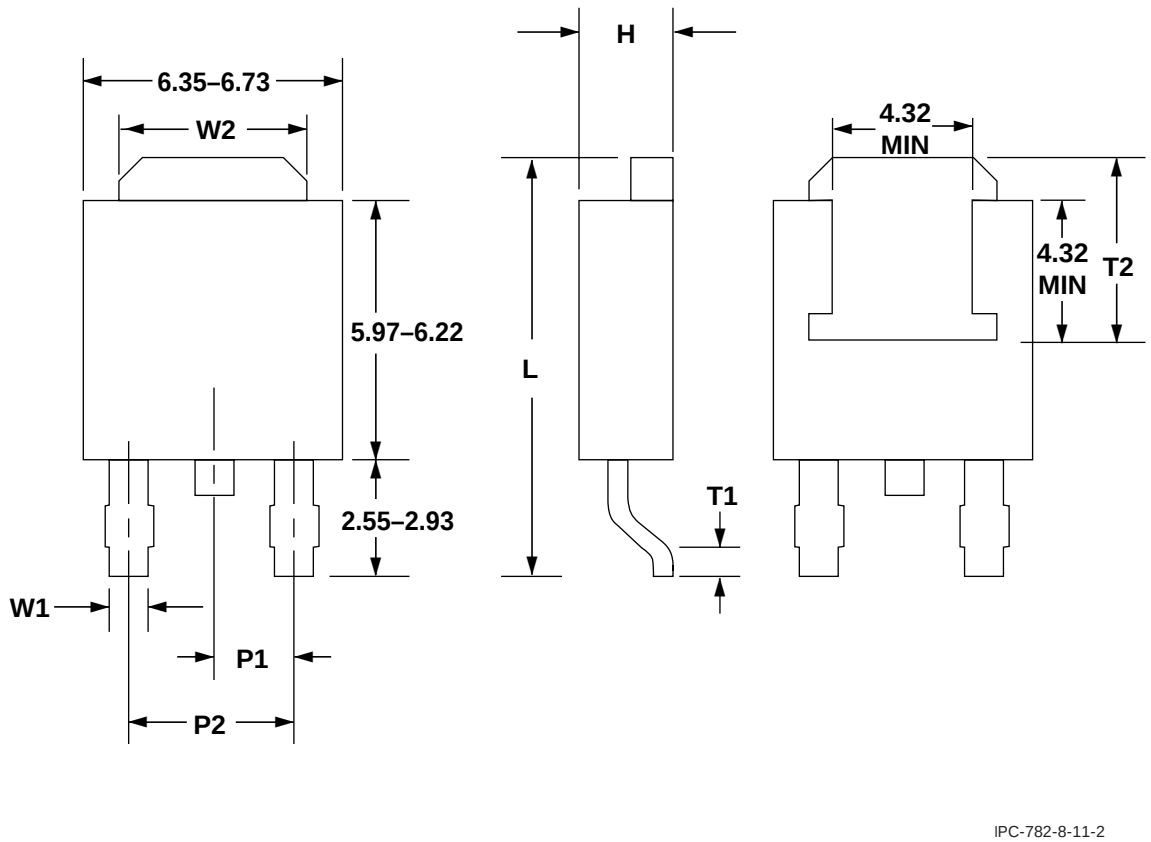
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-252, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a relow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for TO 252 components.



Component Identifier	L		W1		W2		T1		T2		P1	P2	H
	min	max	min	max	min	max	min	max	min	max	basic	basic	max
TS-003*	9.32	10.41	0.64	0.91	4.35	5.35	0.51	0.80	4.00	5.50	2.28	4.57	2.38
TS-005**	14.60	15.88	0.51	0.91	6.22	6.86	2.29	2.79	8.00	9.00	2.54	5.08	4.83
TO 368	18.70	19.10	1.15	1.45	13.30	13.60	2.40	2.70	12.40	12.70	5.45	10.90	5.10

Figure 2 TO 252 component dimensions

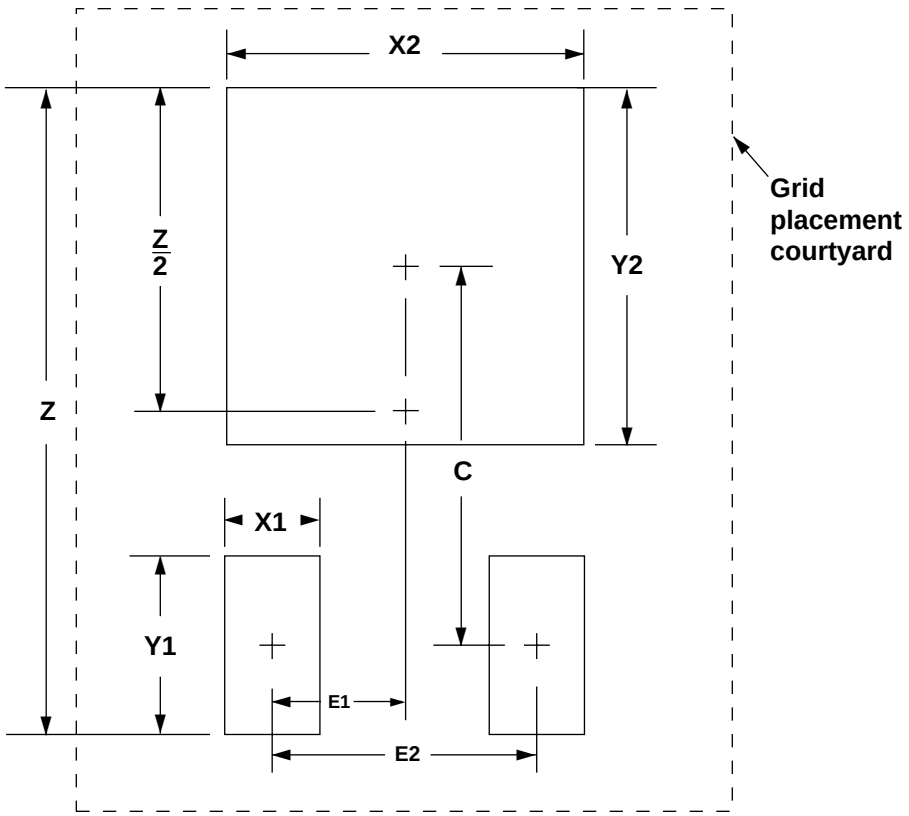
*Formerly TO 252
**Formerly TO 263

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for TO 252 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



Dimensions are in millimeters

IPC-782-8-11-3

RLP No.	Component Identifier	Z (mm)	Y1 (mm)	Y2 (mm)	X1 (mm)	X2 (mm)	C (mm) ref	Placement Grid (No. of Grid Elements)
235A	TS-003*	11.20	1.60	6.20	1.00	5.40	7.30	24x16
236	TS-005**	16.60	3.40	9.60	1.00	6.80	10.10	36x24
237	TO 268	19.80	3.40	13.40	1.40	13.60	11.40	42x34

Figure 3 TO 252 land pattern dimensions

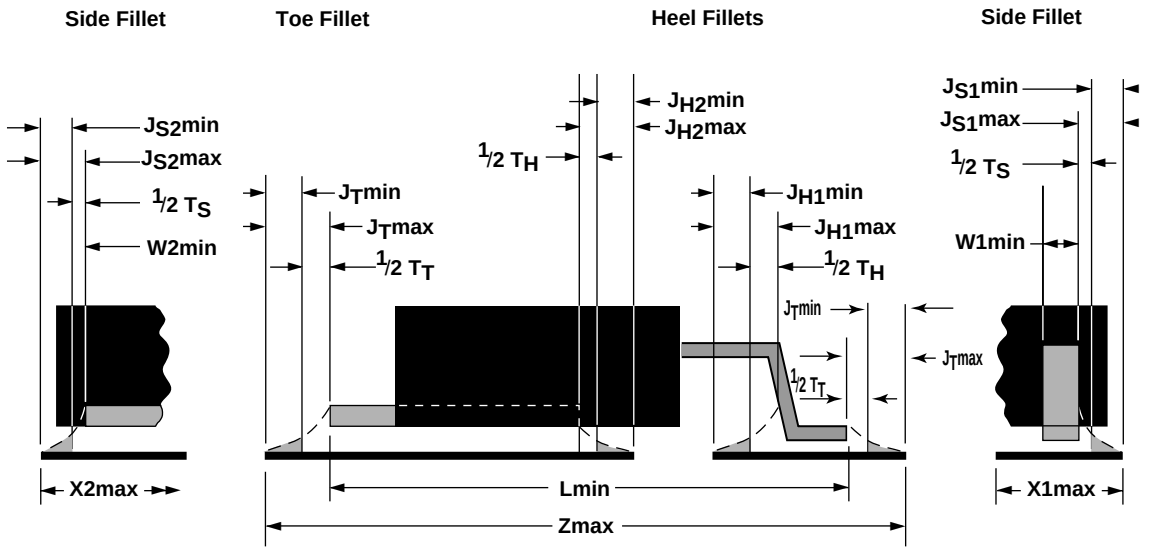
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



IPC-782-8-11-4

RLP No.	Tolerance Assumptions (mm)		Solder Joint															
			Toe (mm)			Heel 1 (mm)			Heel 2 (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_{T1}	J_{H1}min	J_{H1}max	C_{T2}	J_{H2}min	J_{H2}max	C_{W1}	J_{S1}min	J_{S1}max	C_{W1}	J_{S2}min	J_{S2}max
235A	0.10	0.10	1.09	0.39	0.94	0.29	0.37	0.51	1.50	0.29	1.04	0.27	0.03	0.16	1.00	0.02	0.52
236	0.10	0.10	1.28	0.36	1.00	0.50	0.19	0.44	1.00	0.19	0.69	0.40	0.03	0.23	0.64	–0.04	0.28
237	0.10	0.10	0.40	0.34	0.54	0.30	0.27	0.42	0.30	0.27	0.42	0.30	–0.04	0.11	0.30	–0.02	0.13

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**9.0**
Revision	Subject
	Components with Gullwings on Two Sides

1.0 INTRODUCTION This section covers land patterns for components with gullwings on two sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents
Components with Gullwing Leads on Two Sides

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

2.3 Electronic Industries Association of Japan[3]

IC-74-1 General Rules for Preparation of Outline Drawings of Integrated Circuits

IC-74-2 General Rules for Preparation of Outline Drawings of Integrated Circuits, Thin Small Outline Packages

3.0 General Information

3.1 General Component Description The two-sided gull wing family has a number of generic package sizes in the family. The body sizes are varied, but the basic family is characterized by 1.27 mm or 0.63 mm lead centers with leads on the long side of a rectangular body. The family has been expanded to include a limited number of 0.80, 0.65, 0.50, 0.40, and 0.3 mm pitch devices.

Within the component families, body width and lead span are constant, while body length changes as the lead count changes.

A major advantage of this package style is that it can be pretested prior to substrate assembly while still offering relatively high density. Its small area, low height, and minimal weight are its major advantages over DIPs. The package has orientation features on the edge of the package to aid in handling and identification.

Coplanarity is an issue for all components with gullwings on two sides. In general, the leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, (e.g., a granite block), no lead may be more than 0.1 mm off the flat surface.

3.2 Process Considerations Some members of the SOIC family are processed on the secondary side and wave soldered. When parts are processed by wave solder, correct part orientation must be observed. Consult your manufacturer before placing SOIC's on the wave solder side of the board.

High lead count packages and fine pitch parts, 0.63 mm or less, should be processed by infrared reflow, conduction reflow, or hot bar soldering, and should not be wave soldered.

1. Application for copies of EIA and EIAJ documents should be addressed to EIA, 2001 Pennsylvania Ave N.W., Washington, DC, 20006-1813 or Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits (SOIC components) with gullwing leads. Basic construction of the SOIC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

These components are all on 1.27 mm pitch, and are available in narrow body (3.90 mm), wide body (7.50 mm) and extra wide body (8.90 mm) sizes, ranging from 8 to 36 pins.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body and metallic leads.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

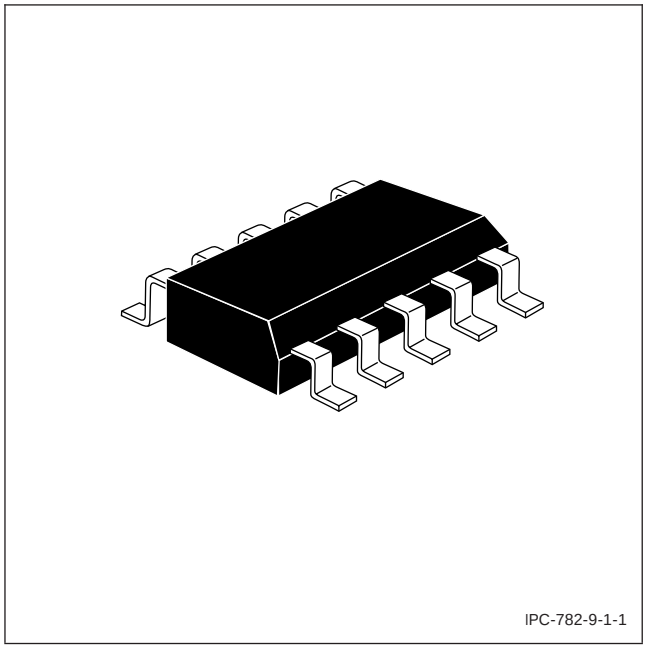


Figure 1 SOIC construction

Solder finish applied over precious-metal leads shall have a diffusion-barrier layer between the lead metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

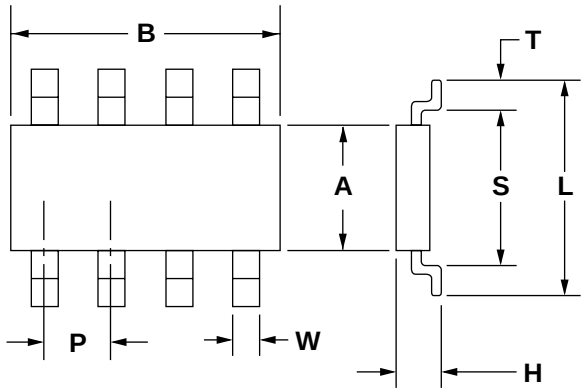
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOIC components.



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Component Identifier	JEDEC Number	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)		P (mm)
		min	max	min	max	min	max	min	max	min	max	min	max	min	max	basic
S08	MS-012 AA	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	4.80	5.00	1.35	1.75	1.27
S08W	—	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	5.05	5.45	2.35	2.65	1.27
S014	MS-012 AB	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	8.55	8.75	1.35	1.75	1.27
S014 W	—	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	8.80	9.20	2.35	2.65	
S016	MS-012 AC	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	9.80	10.00	1.35	1.75	1.27
S016W	MS-013 AA	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	10.10	10.50	2.35	2.65	1.27
S020W	MS-013 AC	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	12.60	13.00	2.35	2.65	1.27
S024W	MO-119 AA	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	15.54	15.85	2.34	2.64	1.27
S024X	MO-120 AA	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	15.54	15.85	2.34	2.64	1.27
S028W	MO-119 AB	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	18.08	18.39	2.34	2.64	1.27
S028X	MO-120 AB	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	18.08	18.39	2.34	2.64	1.27
S032W	MO-119 AC	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	20.62	20.93	2.34	2.64	1.27
S032X	MO-120 AC	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	20.62	20.93	2.34	2.64	1.27
S036W	MO-119 AD	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	23.16	23.47	2.34	2.64	1.27
S036X	MO-120 AD	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	23.16	23.47	2.34	2.64	1.27

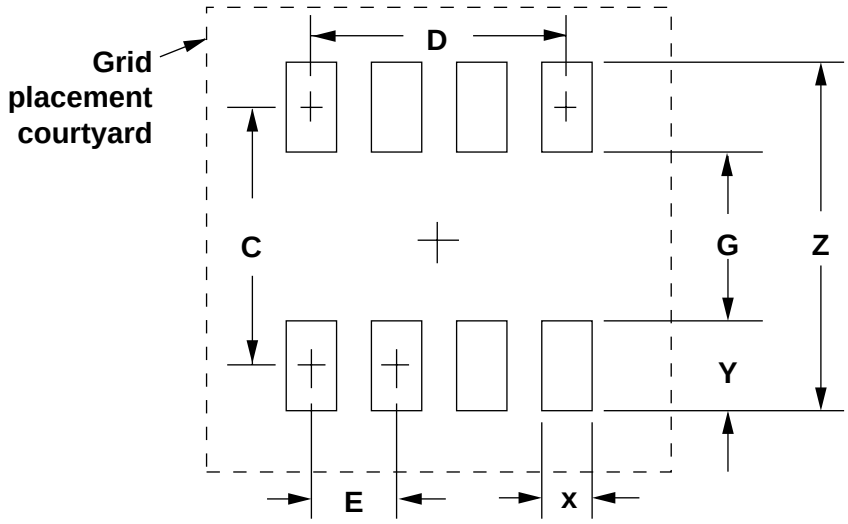
Figure 2 SOIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



IPC-782-9-1-3

RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. Grid Elements)
300A	S08	7.40	3.00	0.60	2.20	5.20	3.81	1.27	16x12
301A	S08W	11.40	7.00	0.60	2.20	9.20	3.81	1.27	24x12
302A	S014	7.40	3.00	0.60	2.20	5.20	7.62	1.27	16x20
303A	S014W	11.40	7.00	0.60	2.20	9.20	7.62	1.27	24x20
304A	S016	7.40	3.00	0.60	2.20	5.20	8.89	1.27	16x22
305A	S016W	11.40	7.00	0.60	2.20	9.20	8.89	1.27	24x22
306A	S020W	11.40	7.00	0.60	2.20	9.20	11.43	1.27	24x28
307A	S024W	11.40	7.00	0.60	2.20	9.20	13.97	1.27	24x32
308A	S024X	13.00	8.60	0.60	2.20	10.80	13.97	1.27	28x32
309A	S028W	11.40	7.00	0.60	2.20	9.20	16.51	1.27	24x38
310A	S028X	13.00	8.60	0.60	2.20	10.80	16.51	1.27	28x38
311A	S032W	11.40	7.00	0.60	2.20	9.20	19.05	1.27	24x44
312A	S032X	13.00	8.60	0.60	2.20	10.80	19.05	1.27	28x44
313A	S036W	11.40	7.00	0.60	2.20	9.20	21.59	1.27	24x48
314A	S036X	13.00	8.60	0.60	2.20	10.80	21.59	1.27	28x48

Figure 3 SOIC land pattern dimensions

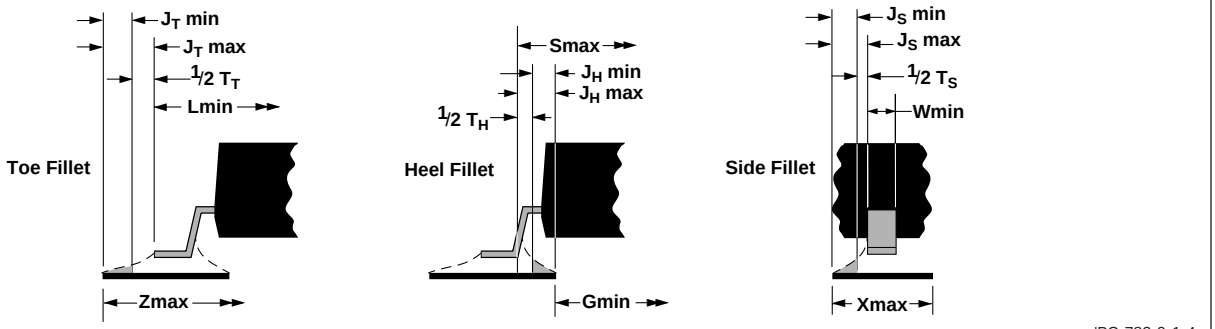
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
300A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
301A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
302A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
303A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
304A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
305A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
306A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
307A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
308A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
309A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
310A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
311A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
312A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
313A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
314A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**9.2**
Revision	Subject
A	**SSOIC**

1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits (SSOIC components) with gullwing leads. Basic construction of the SSOIC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Small Outline Gullead, 12 mm Body, 0.80 mm lead Spacing,'' Outline M0-117, issue ''A,'' and ''Shrink Small Outline Package Family, 7.62 mm body, 0.635 mm,'' Outline MO-018, issue ''A''

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.,
Washington,DC

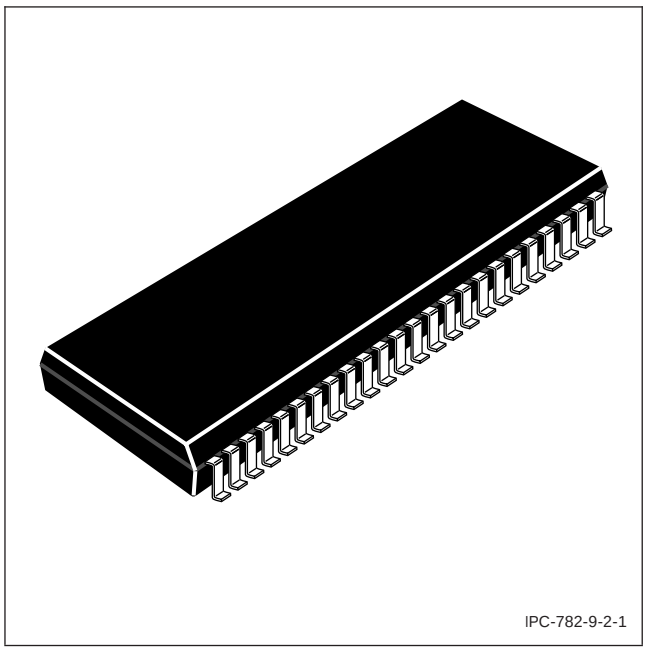


Figure 1 SSOIC construction

3.0 COMPONENT DESCRIPTIONS

These components are all on 0.635 mm pitch, and are available in wide body (7.50 mm) and extra wide body (12.00 mm) sizes, ranging from 48 to 64 pins.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body and metallic leads.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

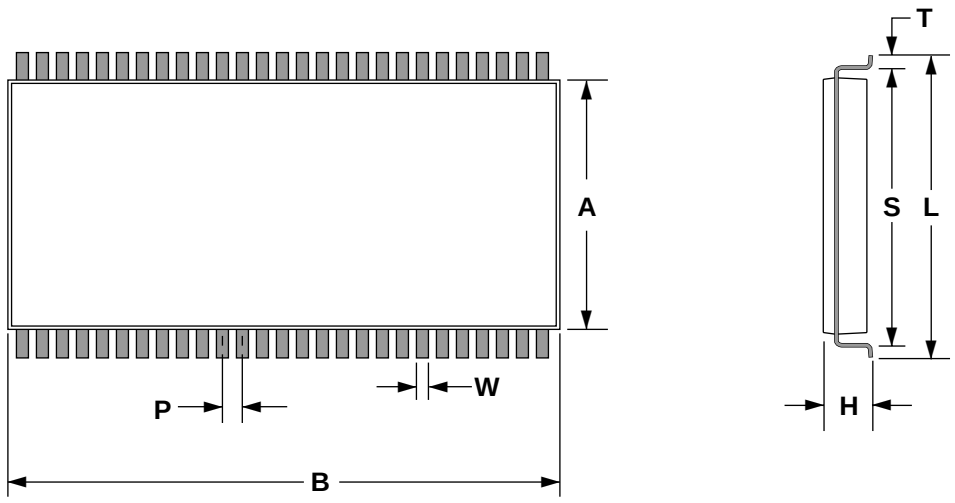
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SSOIC components.



IPC-782-9-2-2

Component Identifier	JEDEC Number	L (mm)		S (mm)		W (mm)		A (mm)		B (mm)		H (mm)		T (mm)		P (mm)
		min	max	min	max	min	max	min	max	min	max	min	max	min	max	basic
SS048	M0118 AA	10.03	10.67	7.99	8.95	0.20	0.30	7.40	7.60	15.75	16.00	2.41	2.20	0.51	1.02	0.635
SS056	M0118 AB	10.03	10.67	7.99	8.95	0.20	0.30	7.40	7.60	18.29	18.54	2.41	2.20	0.51	1.02	0.635
S064	M0117	14.00	14.50	12.40	13.05	0.30	0.45	11.90	12.10	26.17	26.43	1.92	2.00	0.51	0.80	0.800

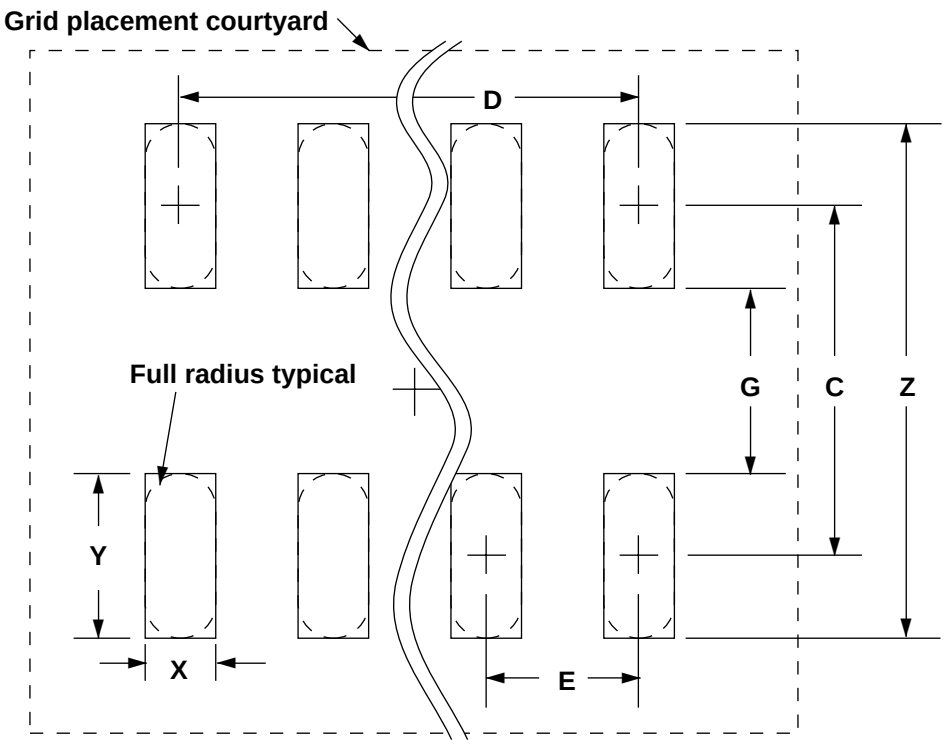
Figure 2 SSOIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SSOIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



IPC-782-9-2-3

RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y ref (mm)	C ref (mm)	D ref (mm)	E ref (mm)	Placement Grid (No. Grid Elements)
330A	SS048	11.60	7.20	0.40	2.20	9.40	14.61	0.64	24x34
331A	SS056	11.60	7.20	0.40	2.20	9.40	17.15	0.64	24x38
332A	S064	15.40	11.40	0.50	2.00	13.40	24.80	0.80	32x54

Figure 3 SSOIC land pattern dimensions

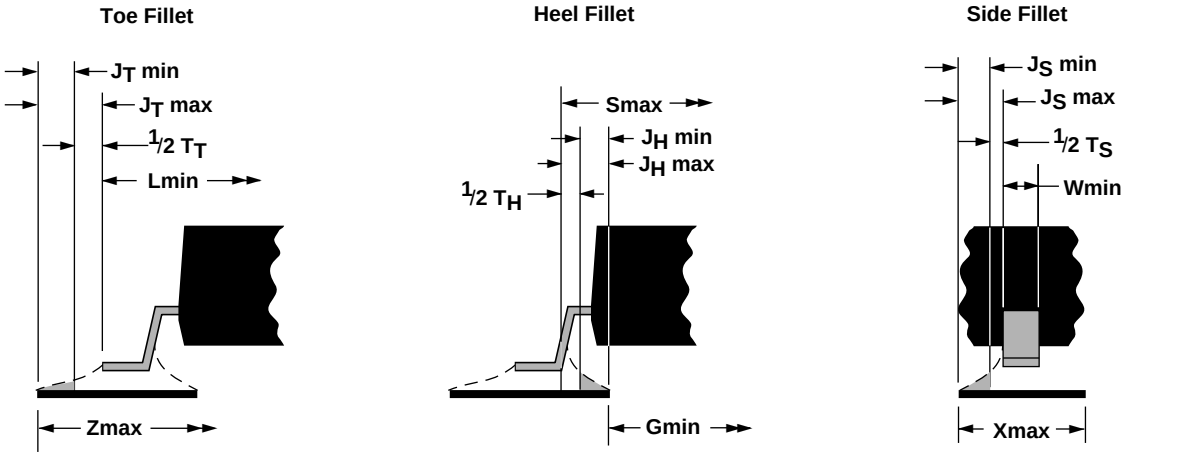
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2JTmin + TT
Where:
JTmin = Minimum toe fillet
TT = Combined tolerances at toe fillet

Gmin = Smax - 2JHmin - TH
Where:
JHmin = Minimum heel fillet
TH = Combined tolerances at heel fillet

Xmax = Wmin + 2JSmin + TS
Where:
JSmin = Minimum side fillet
TS = Combined tolerances at side fillet

IPC-782-9-2-4

	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$T_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
330A	0.10	0.10	0.64	0.46	0.79	0.96	0.39	0.88	0.10	0.01	0.10
331A	0.10	0.10	0.64	0.46	0.79	0.96	0.39	0.88	0.10	0.01	0.10
332A	0.10	0.10	0.50	0.44	0.70	0.65	0.49	0.82	0.15	0.00	0.10

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**9.3**
Revision	Subject
A	**SOP**

1.0 SCOPE

This subsection provides component and land pattern dimensions for small outline packages (SOP components) with gullwing leads on two sides. Basic construction of the SOP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association of Japan (EIAJ)

EIAJ-7402-1 General Rules for the Preparation of Outine Drawings of Integrated Circuits Small Outline Packages

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction IPC-SM-782 has defined center-to-center spacing for the land pattern slightly differently than is indicated in the EIAJ specification ED 7402-1.

This specification allows for 6 families of the SOP. EIAJ classifies the families by the center-to-center distance of the land patterns and the outer extremities of the leads (dimension ''L'' in IPC-SM-782). The basic construction of the SOP specified by EIAJ is the same construction as for SOIC specified by JEDEC. Both have gullwing leads on 1.27 mm centers.

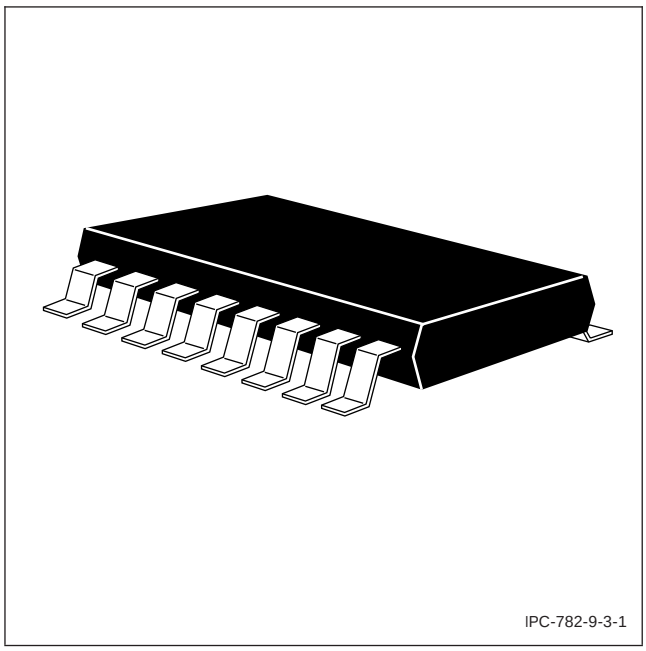


Figure 1 SOPIC construction

The EIAJ specification allows for a number of positions of the components to be in any of the families (e.g., body width). The sizes shown in Figure 2 are the most common, however, there are Type II SOP 14s and there are also Type I SOP 16s. See Figure 2.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

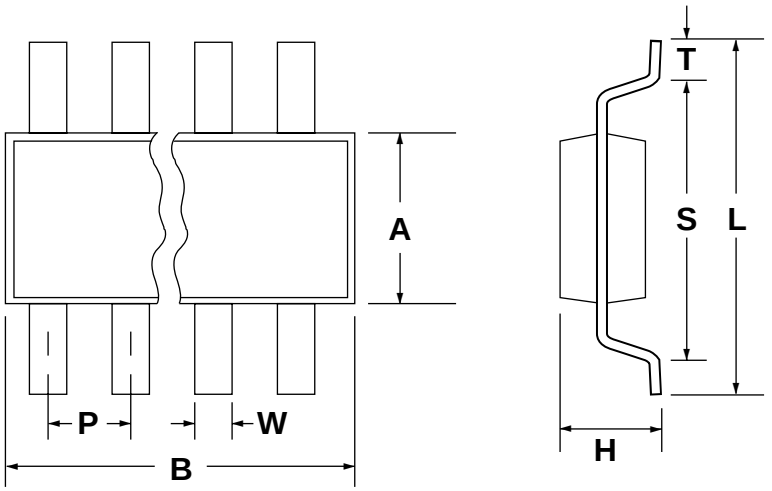
3.1.2 Marking Parts are available with or without part number markings. Usually an index mark indicates pin 1.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Solder Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOPIC components.



IPC-782-9-3-2

Component Identifier (mm)	Type	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)	H (mm)	P (mm)
		min	max	min	max	min	max	min	max	min	max	max	max	basic
SOP 6	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	6.35	1.5	1.27
SOP 8	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	6.35	1.5	1.27
SOP 10	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	8.89	1.5	1.27
SOP 12	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	8.89	1.5	1.27
SOP 14	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	11.43	1.5	1.27
SOP 16	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	11.43	2.0	1.27
SOP 18	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	13.97	2.0	1.27
SOP 20	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	13.97	2.0	1.27
SOP 22	III	9.53	10.80	7.53	8.92	0.35	0.51	0.60	1.00	6.33	8.13	16.51	2.5	1.27
SOP 24	III	9.53	10.80	7.53	8.92	0.35	0.51	0.60	1.00	6.33	8.13	16.51	2.5	1.27
SOP 28	IV	11.43	12.70	9.43	10.82	0.35	0.51	0.60	1.00	8.23	10.03	19.05	3.0	1.27
SOP 30	IV	11.43	12.70	9.43	10.82	0.35	0.51	0.60	1.00	8.23	10.03	21.59	3.0	1.27
SOP 32	V	13.34	14.61	11.34	12.73	0.35	0.51	0.60	1.00	10.14	11.94	21.59	3.5	1.27
SOP 36	V	13.34	14.61	11.34	12.73	0.36	0.51	0.60	1.00	10.14	11.94	24.13	3.5	1.27
SOP 40	VI	15.24	16.51	13.24	14.63	0.35	0.51	0.60	1.00	12.04	13.84	27.94	4.0	1.27
SOP 42	VI	15.24	16.51	13.24	14.63	0.35	0.51	0.60	1.00	12.04	13.84	27.94	4.0	1.27

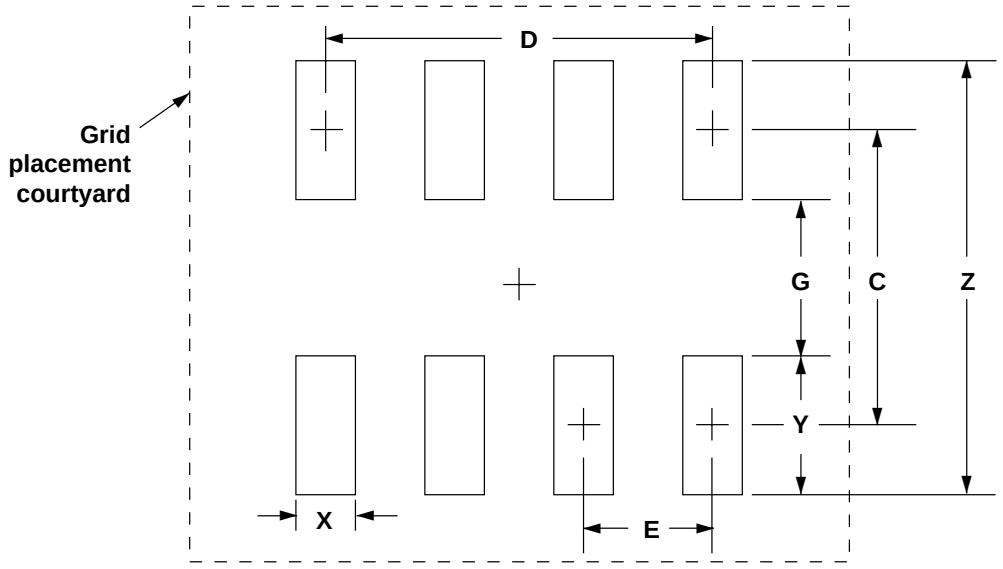
Figure 2 SOPIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOPIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. Grid Elements)
360A	SOP 6	7.40	3.00	0.60	2.20	5.20	2.54	1.27	16x14
361A	SOP 8	7.40	3.00	0.60	2.20	5.20	3.81	1.27	16x14
362A	SOP 10	7.40	3.00	0.60	2.20	5.20	5.08	1.27	16x18
363A	SOP 12	7.40	3.00	0.60	2.20	5.20	6.35	1.27	16x18
364A	SOP 14	7.40	3.00	0.60	2.20	5.20	7.62	1.27	16x24
365A	SOP 16	9.40	5.00	0.60	2.20	7.20	8.89	1.27	20x24
366A	SOP 18	9.40	5.00	0.60	2.20	7.20	10.16	1.27	20x28
367A	SOP 20	9.40	5.00	0.60	2.20	7.20	11.43	1.27	20x28
368A	SOP 22	11.20	6.80	0.60	2.20	9.00	13.97	1.27	24x34
369A	SOP 24	11.20	6.80	0.60	2.20	9.00	13.97	1.27	24x34
370A	SOP 28	13.20	8.80	0.60	2.20	11.00	16.51	1.27	28x40
371A	SOP 30	13.20	8.80	0.60	2.20	11.00	17.78	1.27	28x44
372A	SOP 32	15.00	10.60	0.60	2.20	12.80	19.05	1.27	32x44
373A	SOP 36	15.00	10.60	0.60	2.20	12.80	21.59	1.27	32x50
374A	SOP 40	17.00	12.60	0.60	2.20	14.80	24.13	1.27	36x56
375A	SOP 42	17.00	12.60	0.60	2.20	14.80	25.40	1.27	36x56

Figure 3 SOPIC land pattern dimensions

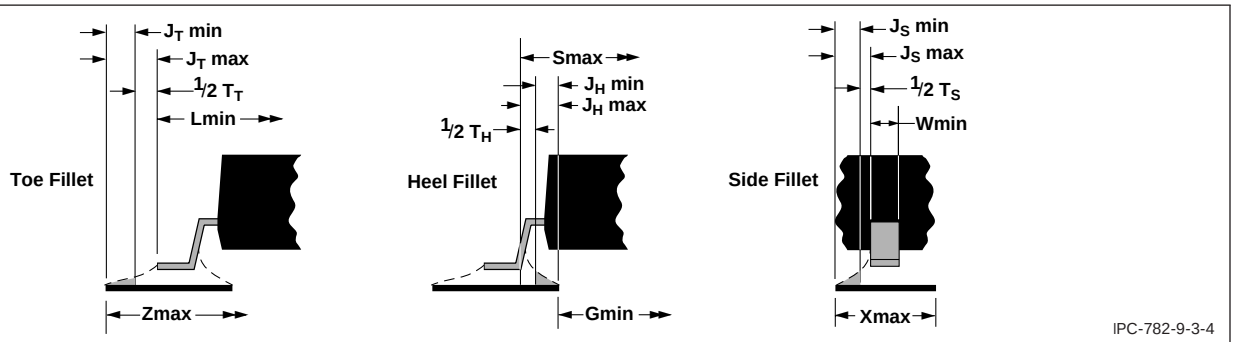
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
360A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
361A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
362A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
363A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
364A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
365A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
366A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
367A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
368A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
369A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
370A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
371A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
372A	0.10	0.10	1.27	0.19	0.83	1.26	0.37	1.07	0.16	0.02	0.13
373A	0.10	0.10	1.27	0.19	0.83	1.26	0.37	1.07	0.16	0.02	0.13
374A	0.10	0.10	1.27	0.24	0.88	1.26	0.32	1.02	0.16	0.02	0.13
375A	0.10	0.10	1.27	0.24	0.88	1.26	0.32	1.02	0.16	0.02	0.13

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for thin small outline packages (TSOP components) with gullwing leads on two sides. Basic construction of the TSOP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7402-3 General Rules for the Preparation of Outline Drawings of Integrated Circuits Thin Small Outline Packages

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction The TSOP package is unique among the component families of this section becaue its leads protrude from the short side of the plastic body. The TSOP components are available in four different pitches: 0.3, 0.4, 0.5, and 0.65 mm. They are typically specified by their two largest dimensions—the plastic body size (in the short dimension), and the nominal toe-to-toe length (in the long dimension). Their use has grown because their height (less than 1.27 mm) allows them to be used in memory card technology.

EIAJ ED-7402-3 outlines sixteen different body sizes with pin counts ranging from 16–76 pins. In general, as the long dimension increases, the pitch decreases. See Figure 1.

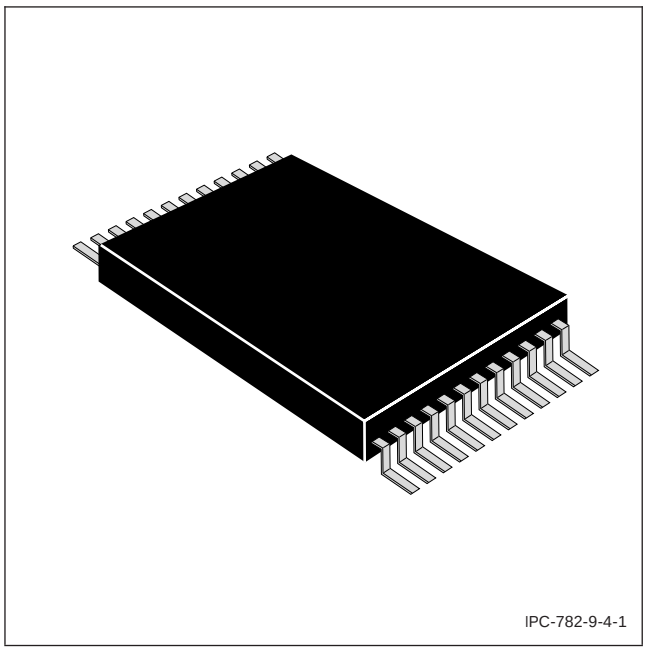


Figure 1 TSOP construction

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

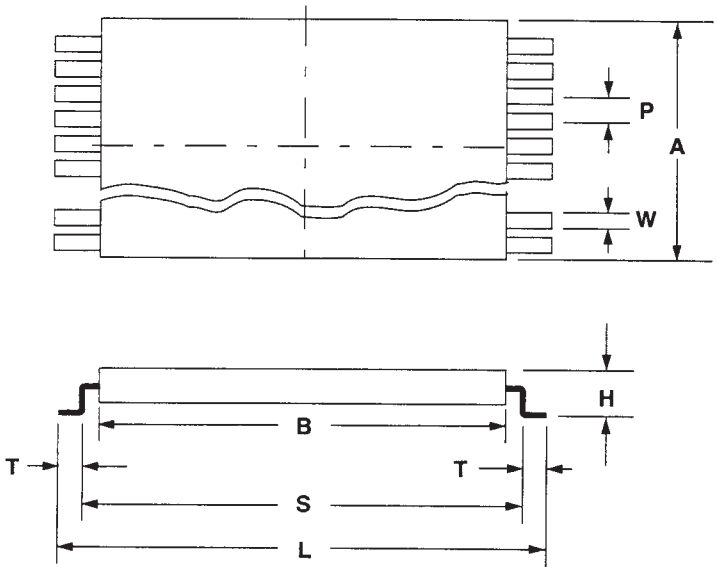
3.1.2 Marking Parts are available with or without part number markings. Usually an index mark indicates pin 1.

3.1.3 Carrier Packages Format Trays are usually used for handling TSOP's.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for TSOP components.



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Component Identifier (mm)	Pin Count	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
		min	max	min	max	min	max	m in	max	min	max	min	max	max	basic
TSOP 6x14	16	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	5.80	6.20	12.20	12.60	1.27	0.65
TSOP 6x16	24	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	5.80	6.20	14.20	14.60	1.27	0.50
TSOP 6x18	28	17.80	18.20	16.40	16.78	0.05	0.22	0.40	0.70	5.80	6.20	16.20	16.60	1.27	0.40
TSOP 6x20	36	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	5.80	6.20	18.20	18.60	1.27	0.30
TSOP 8x14	24	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	7.80	8.20	12.20	12.60	1.27	0.65
TSOP 8x16	32	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	7.80	8.20	14.20	14.60	1.27	0.50
TSOP 8x18	40	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	7.80	8.20	16.20	16.60	1.27	0.40
TSOP 8x20	52	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	7.80	8.20	18.20	18.60	1.27	0.30
TSOP 10x14	28	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	9.80	10.20	12.20	12.60	1.27	0.65
TSOP 10x16	40	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	9.80	10.20	14.20	14.60	1.27	0.50
TSOP 10x18	48	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	9.80	10.20	16.20	16.60	1.27	0.40
TSOP 10x20	64	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	9.80	10.20	18.20	18.60	1.27	0.30
TSOP 12x14	36	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	11.80	12.20	12.20	12.60	1.27	0.65
TSOP 12x16	48	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	11.80	12.20	14.20	14.60	1.27	0.50
TSOP 12x18	60	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	11.80	12.20	16.20	16.60	1.27	0.40
TSOP 12x20	76	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	11.80	12.20	18.20	18.60	1.27	0.30

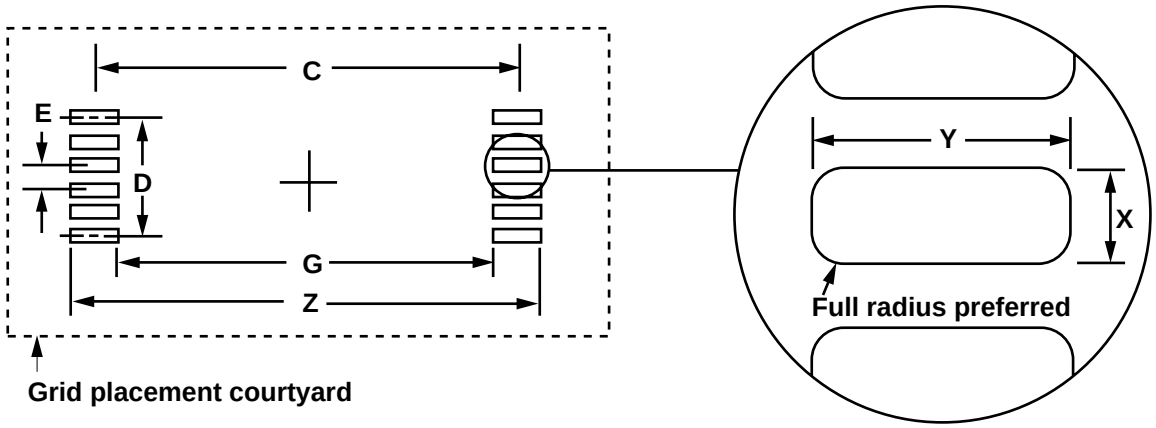
Figure 2 TSOP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for TSOP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Pin Count	Placement Grid (No. of Grid Elements)
390A	6x14	14.80	11.60	0.40	1.60	13.20	4.55	0.65	16	14x32
391A	6x16	16.80	13.60	0.30	1.60	15.20	5.50	0.50	24	14x36
392A	6x18	18.80	15.60	0.25	1.60	17.20	5.20	0.40	28	14x40
393A	6x20	20.80	17.60	0.17	1.60	19.20	5.10	0.30	36	14x44
394A	8x14	14.80	11.60	0.40	1.60	13.20	7.15	0.65	24	18x32
395A	8x16	16.80	13.60	0.30	1.60	15.20	7.50	0.50	32	18x36
396A	8x18	18.80	15.60	0.25	1.60	17.20	7.60	0.40	40	18x40
397A	8x20	20.80	17.60	0.17	1.60	19.20	7.50	0.30	52	18x44
398A	10x14	14.80	11.60	0.40	1.60	13.20	8.45	0.65	28	22x32
399A	10x16	16.80	13.60	0.30	1.60	15.20	9.50	0.50	40	22x36
400A	10x18	18.80	15.60	0.25	1.60	17.20	9.20	0.40	48	22x40
401A	10x20	20.80	17.60	0.17	1.60	19.20	9.30	0.30	64	22x44
402A	12x14	14.80	11.60	0.40	1.60	13.20	11.05	0.65	36	26x32
403A	12x16	16.80	13.60	0.30	1.60	15.20	11.50	0.50	48	26x36
404A	12x18	18.80	15.60	0.25	1.60	17.20	11.60	0.40	60	26x40
405A	12x20	20.80	17.60	0.17	1.60	19.20	11.10	0.30	76	26x44

Figure 3 TSOP land pattern dimensions

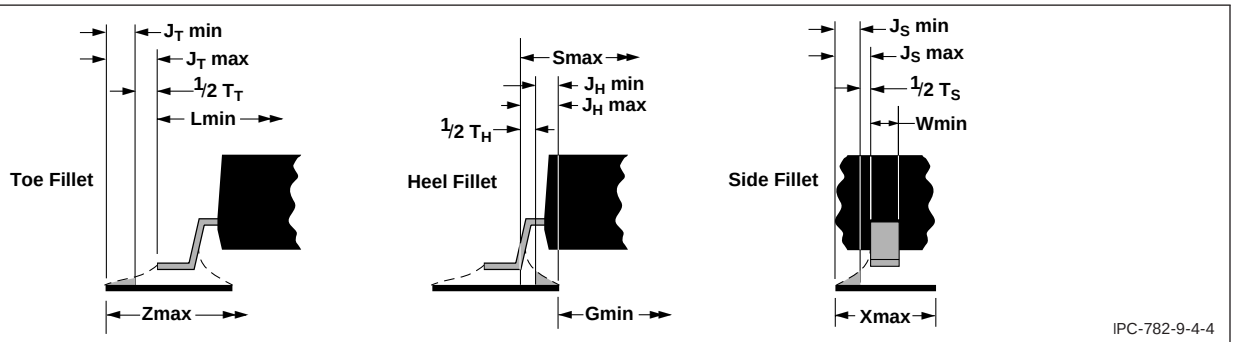
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
390A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
391A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
392A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.01	0.10
393A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.06	-0.03	0.06
394A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
395A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
396A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
397A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06
398A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
399A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
400A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
401A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06
402A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
403A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
404A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
405A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for ceramic flat packs (CFP components) with gullwing leads on two sides. Basic construction of the CFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:

Outline	*Issues*	*Title*
MO-003	C	Flatpack Family, 5.08 Width, 1.27 Pitch
MO-004	C	Flatpack Family, 7.62 Width, 1.27 Pitch
MO-018	—	Flatpack Family, 10.16 Width, 1.27 Pitch
MO-019	D	Flatpack Family, 10.16 Width, 1.27 Pitch
MO-020	C	Flatpack Family, 12.70 Width, 1.27 Pitch
MO-021	C	Flatpack Family, 15.24 Width, 1.27 Pitch
MO-022	D	Flatpack Family, 17.78 Width, 1.27 Pitch
MO-023	C	Flatpack Family, 22.86 Width, 1.27 Pitch

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Basic construction consists of a ceramic body and metallic leads. Leads are trimmed and formed into gullwing shape as shown in Figure 2.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier trays are used for handling CFPs.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

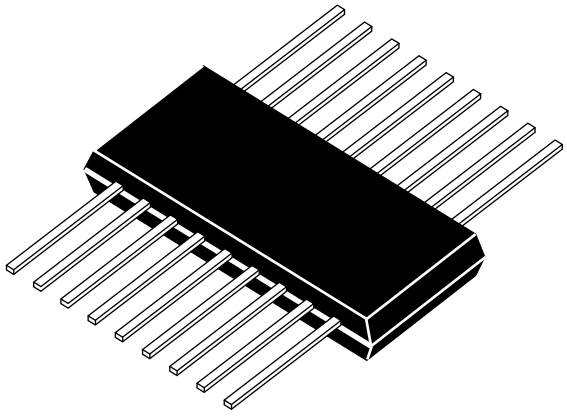


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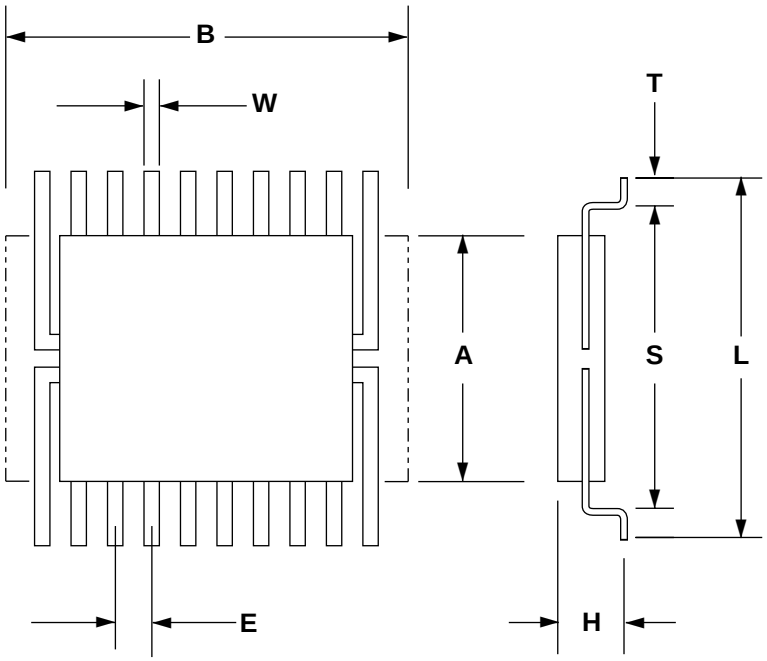
Figure 1 CFP construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for CFP components.



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CFP Component Identifier	Pin Count	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)	H (mm)	E
		min	max	min	max	min	max	min	max	min	max	max	max	basic
MO-003	10	9.00	9.60	6.46	7.26	0.25	0.35	0.90	1.27	2.54	5.08	7.36	2.50	1.27
MO-003	14	9.00	9.60	6.46	7.26	0.25	0.35	0.90	1.27	2.54	5.08	9.90	2.50	1.27
MO-004	10	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	7.36	2.50	1.27
MO-004	14	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	9.90	2.50	1.27
MO-004	16	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	11.17	2.50	1.27
MO-018	20	11.00	11.60	8.46	9.26	0.25	0.35	0.90	1.27	7.62	10.16	13.71	2.50	1.27
MO-019	24	15.00	15.60	12.46	13.26	0.38	0.48	0.90	1.27	7.62	10.16	16.25	2.50	1.27
MO-019	28	15.00	15.60	12.46	13.26	0.46	0.56	0.90	1.27	7.62	10.16	18.79	2.50	1.27
MO-020	36	17.00	17.60	14.46	15.26	0.38	0.48	0.90	1.27	10.16	12.70	23.87	3.00	1.27
MO-020	40	17.00	17.60	14.46	15.26	0.33	0.43	0.90	1.27	10.16	12.70	26.41	3.00	1.27
MO-021	16	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	11.17	2.50	1.27
MO-021	24	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	16.25	2.50	1.27
MO-021	36	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	23.87	3.00	1.27
MO-022	20	22.00	22.60	19.46	20.26	0.38	0.48	0.90	1.27	15.24	17.78	13.71	2.50	1.27
MO-022	42	22.00	22.60	19.46	20.26	0.46	0.56	0.90	1.27	15.24	17.78	27.68	3.00	1.27
MO-023	36	27.00	27.60	24.46	25.26	0.38	0.48	0.90	1.27	20.32	22.86	23.87	3.00	1.27
MO-023	50	27.00	27.60	24.46	25.26	0.38	0.48	0.90	1.27	20.32	22.86	32.76	3.00	1.27

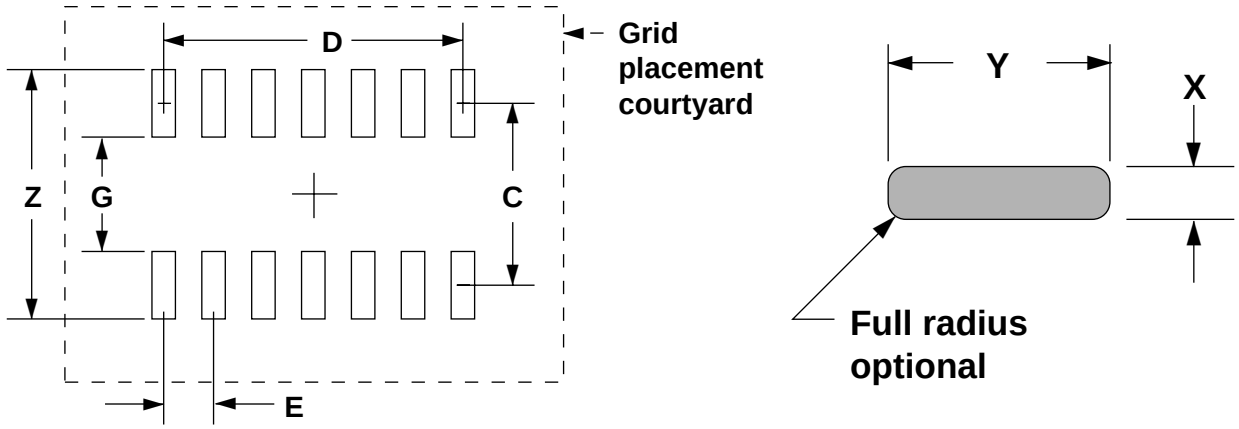
Figure 2 CFP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for CFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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RLP No.	Component Identifier	Pin Count	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. Grid Elements)
420	MO-003	10	10.20	6.00	0.65	2.20	8.0	5.08	1.27	22x16
421	MO-003	14	10.20	6.00	0.65	2.20	8.0	7.62	1.27	22x22
422	MO-004	10	12.20	8.00	0.65	2.20	10.0	5.08	1.27	26x16
423	MO-004	14	12.20	8.00	0.65	2.20	10.0	7.62	1.27	26x22
424	MO-004	16	12.20	8.00	0.65	2.20	10.0	8.89	1.27	26x24
425	MO-018	20	12.20	8.00	0.65	2.20	10.0	11.43	1.27	26x28
426	MO-019	24	16.20	12.00	0.65	2.20	14.0	13.97	1.27	34x34
427	MO-019	28	16.20	12.00	0.65	2.20	14.0	16.51	1.27	34x38
428	MO-020	36	18.20	14.00	0.65	2.20	16.0	21.59	1.27	38x48
429	MO-020	40	18.20	14.00	0.65	2.20	16.0	24.13	1.27	38x54
430	MO-021	16	21.20	17.00	0.65	2.20	19.0	8.89	1.27	44x24
431	MO-021	24	21.20	17.00	0.65	2.20	19.0	13.97	1.27	44x34
432	MO-021	36	21.20	17.00	0.65	2.20	19.0	21.59	1.27	44x48
433	MO-022	20	23.20	19.00	0.65	2.20	21.0	11.43	1.27	48x28
434	MO-022	42	23.20	19.00	0.65	2.20	21.0	25.40	1.27	48x56
435	MO-023	36	28.20	24.00	0.65	2.20	26.0	21.59	1.27	58x48
436	MO-023	50	28.20	24.00	0.65	2.20	26.0	30.48	1.27	58x66

Figure 3 CFP land pattern dimensions

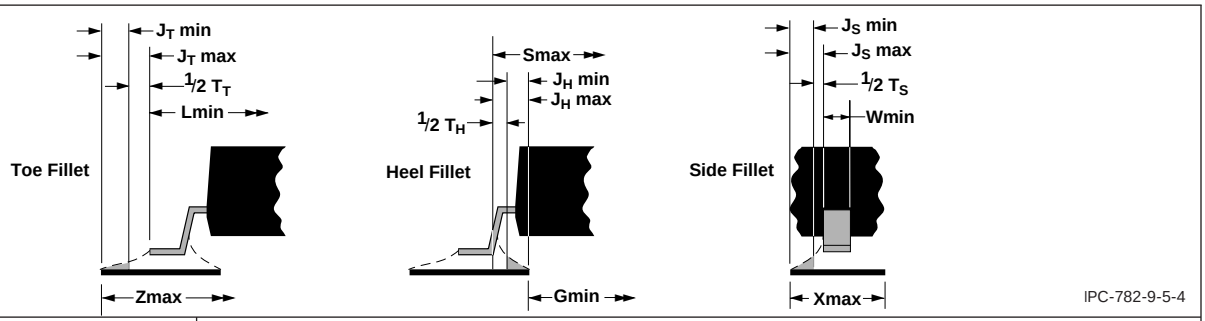
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$T_S$min	$T_S$max
420	0.2	0.2	0.60	0.27	0.60	0.60	0.30	0.73	0.10	0.05	0.20
421	0.2	0.2	0.60	0.27	0.60	0.60	0.30	0.73	0.10	0.05	0.20
422	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.08	–0.02	0.14
423	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
424	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
425	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	0.05	0.20
426	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
427	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.06	0.10
428	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
429	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	0.01	0.16
430	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
431	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
432	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
433	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
434	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.06	0.10
435	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
436	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14

Figure 4 Tolerance and solder joint analysis

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Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**10.0**
Revision	Subject
	Components with J Leads on Two Sides

1.0 INTRODUCTION This section covers land patterns for components with J leads on two sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:
MO-077, issue ''C,'' dated 8/91
MO-065, issue ''A,'' dated 5/87
MO-063, issue ''A,'' dated 4/2/87
MO-061, issue ''C,'' date 8/91

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7406 General Rules for the Preparation of Outline Drawings of Integrated Circuits

2.3 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description This section provides the component and land pattern dimensions for small outline integrated circuits with ''J'' leads (SOJ components). Basic construction of the SOJ device is also covered. At the end of the subsections are listings of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

3.2 Packaging Components may be provided in tube or tape packaging. Tape is preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity requirements required for placement and soldering. EIA-481 provides details on tape requirements.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits with ''J'' leads (SOJ components). Basic construction of the SOJ device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 10.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

The two-sided J lead family is a small outline family identified by the dimension of the body size in inches. For example, the SOJ/300 has a body size of 0.300 inches or 7.63 mm, the SOJ/350 has a body size of 0.350 inches or 8.88 mm, the SOJ/400 has a body size of 0.400 inches or 10.12 mm, and the SOJ/450 has a body size of 0.450 inches or 11.38 mm. Package lead counts range from 14 to 28 pins.

The small-outline ''J'' (SOJ) package has leads on two sides, similar to a DIP. The lead configuration, like the letter J, extends out the side of the package and bends under the package forming a J bend. The point of contact of the lead to the land pattern is at the apex of the J bend and is the basis for the span of the land pattern.

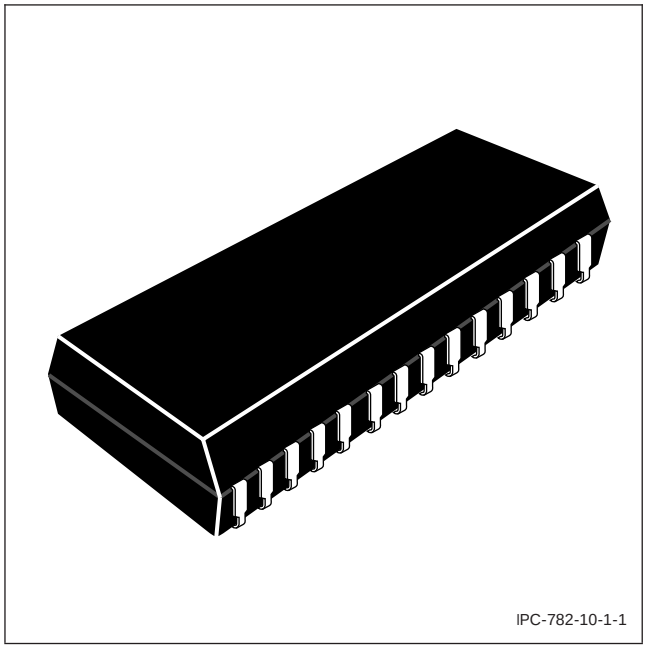

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Figure 1 SOJ construction

The leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, no lead may be more than 0.1 mm off the flat surface.

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory IC's are often used in multiples, and buss lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of ''J'' leads. With high capacity memory systems, the space savings can be significant.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body, and metallic ''J'' leads.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% lead. Solder may be applied to theleads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finishshould be at least 0l.0075 mm [0.0003 in] thick.

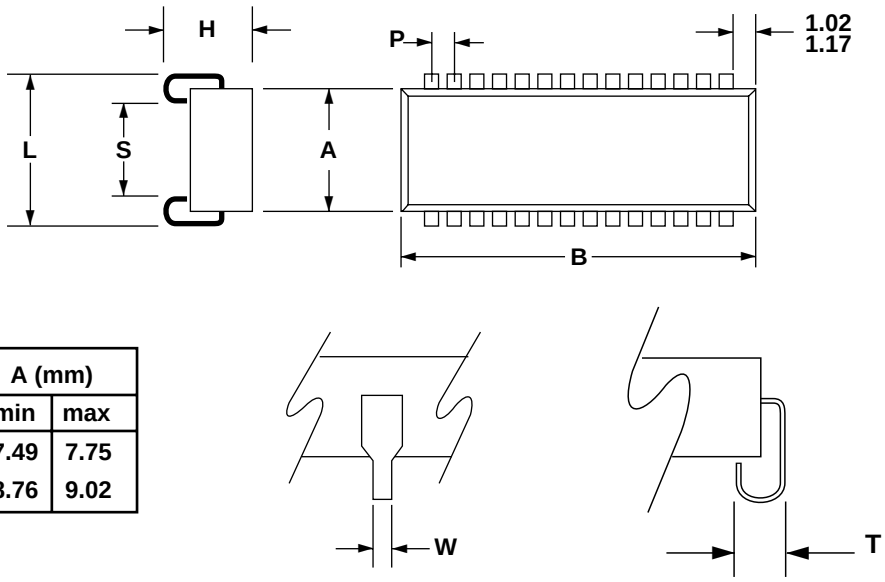
3.1.2 Marking The SOIC family of parts is generally marked with manufacturers part numbers, manufacturers name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/manufacturing lot and/or manufacturing location.

3.1.3 Carrier Package Format Components may be provided in tube or tape packaging. Tape is preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity requirements required for placement and soldering. EIA-481 provides details on tape requirements.

3.1.4 Process Considerations J lead packages are normally processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

In this subsection, Figures 2a–2b provide the component dimensions for SOJ components. (Also see page 4.)



A (in.)	A (mm)	
ref.	min	max
0.300	7.49	7.75
0.350	8.76	9.02

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Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	m in	max	max	basic
SOJ 14/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	12.19	12 .50	3.75	1.27
SOJ 20/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27
SOJ 14/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27

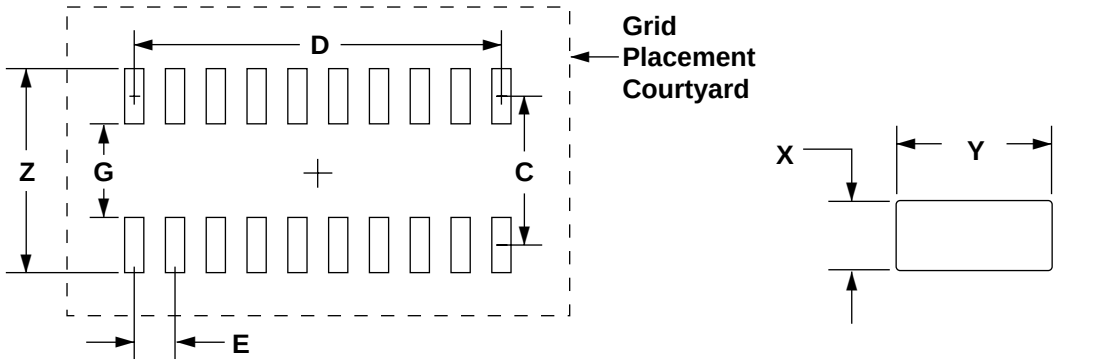
Figure 2a SOJ component dimensions

5.0 LAND PATTERN DIMENSIONS

In this subsection, Figures 3a–3b provide the land pattern dimensions for SOJ components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns. (Also see page 5.)

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 6. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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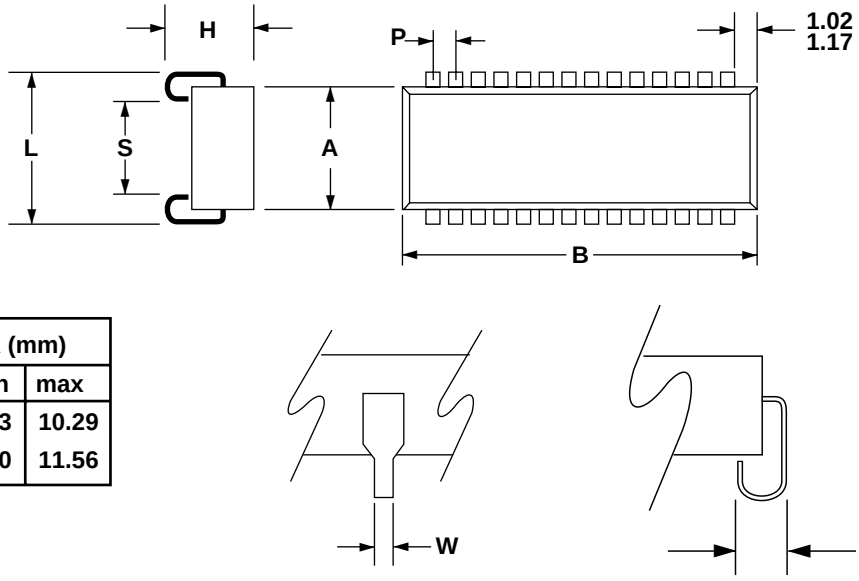
RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) basic	E (mm) basic	Placement Grid (No. Grid Elements)
480A	SOJ 14/300	9.40	5.00	0.60	2.20	7.20	7.62	1.27	20x22
481A	SOJ 16/300	9.40	5.00	0.60	2.20	7.20	8.89	1.27	20x24
482A	SOJ 18/300	9.40	5.00	0.60	2.20	7.20	10.16	1.27	20x26
483A	SOJ 20/300	9.40	5.00	0.60	2.20	7.20	11.43	1.27	20x28
484A	SOJ 22/300	9.40	5.00	0.60	2.20	7.20	12.70	1.27	20x32
485A	SOJ 24/300	9.40	5.00	0.60	2.20	7.20	13.97	1.27	20x34
486A	SOJ 26/300	9.40	5.00	0.60	2.20	7.20	15.24	1.27	20x36
487A	SOJ 28/300	9.40	5.00	0.60	2.20	7.20	16.51	1.27	20x38
490A	SOJ 14/350	10.60	6.20	0.60	2.20	8.40	7.62	1.27	24x22
491A	SOJ 16/350	10.60	6.20	0.60	2.20	8.40	8.89	1.27	24x24
492A	SOJ 18/350	10.60	6.20	0.60	2.20	8.40	10.16	1.27	24x26
493A	SOJ 20/350	10.60	6.20	0.60	2.20	8.40	11.43	1.27	24x28
494A	SOJ 22/350	10.60	6.20	0.60	2.20	8.40	12.70	1.27	24x32
495A	SOJ 24/350	10.60	6.20	0.60	2.20	8.40	13.97	1.27	24x34
496A	SOJ 26/350	10.60	6.20	0.60	2.20	8.40	15.24	1.27	24x36
497A	SOJ 28/350	10. 60	6.20	0.60	2.20	8.40	16.51	1.27	24x38

Figure 3a SOJ land pattern dimensions



A (in.)	A (mm)	
ref.	min	max
0.400	10.03	10.29
0.450	11.30	11.56

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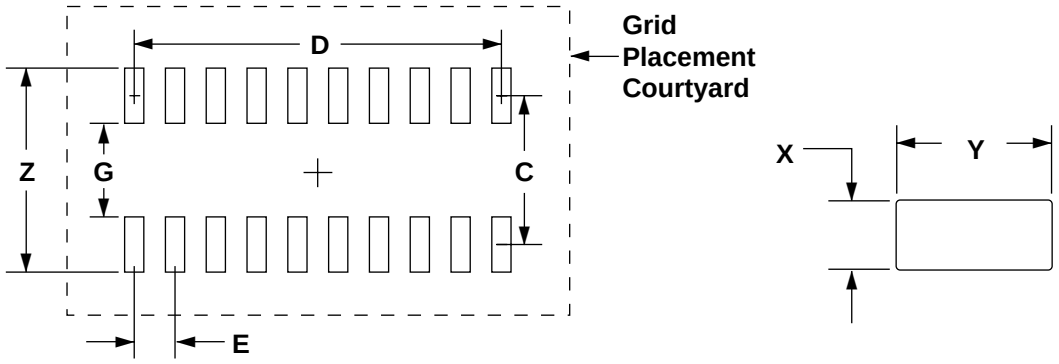
Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	max	basic
SOJ 14/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27
SOJ 14/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27

Figure 2b SOJ component dimensions



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RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) basic	E (mm) basic	Placement Grid (No. Grid Elements)
500A	SOJ 14/400	11.80	7.40	0.60	2.20	9.60	7.62	1.27	26x22
501A	SOJ 16/400	11.80	7.40	0.60	2.20	9.60	8.89	1.27	26x24
502A	SOJ 18/400	11.80	7.40	0.60	2.20	9.60	10.16	1.27	26x26
503A	SOJ 20/400	11.80	7.40	0.60	2.20	9.60	11.43	1.27	26x28
504A	SOJ 22/400	11.80	7.40	0.60	2.20	9.60	12.70	1.27	26x32
505A	SOJ 24/400	11.80	7.40	0.60	2.20	9.60	13.97	1.27	26x34
506A	SOJ 26/400	11.80	7.40	0.60	2.20	9.60	15.24	1.27	26x36
507A	SOJ 28/400	11.80	7.40	0.60	2.20	9.60	16.51	1.27	26x38
510A	SOJ 14/450	13.20	8.80	0.60	2.20	11.00	7.62	1.27	28x22
511A	SOJ 16/450	13.20	8.80	0.60	2.20	11.00	8.89	1.27	28x24
512A	SOJ 18/450	13.20	8.80	0.60	2.20	11.00	10.16	1.27	28x26
513A	SOJ 20/450	13.20	8.80	0.60	2.20	11.00	11.43	1.27	28x28
514A	SOJ 22/450	13.20	8.80	0.60	2.20	11.00	12.70	1.27	28x32
515A	SOJ 24/450	13.20	8.80	0.60	2.20	11.00	13.97	1.27	28x34
516A	SOJ 26/450	13.20	8.80	0.60	2.20	11.00	15.24	1.27	28x36
517A	SOJ 28/450	13.20	8.80	0.60	2.20	11.00	16.51	1.27	28x38

Figure 3b SOJ land pattern dimensions

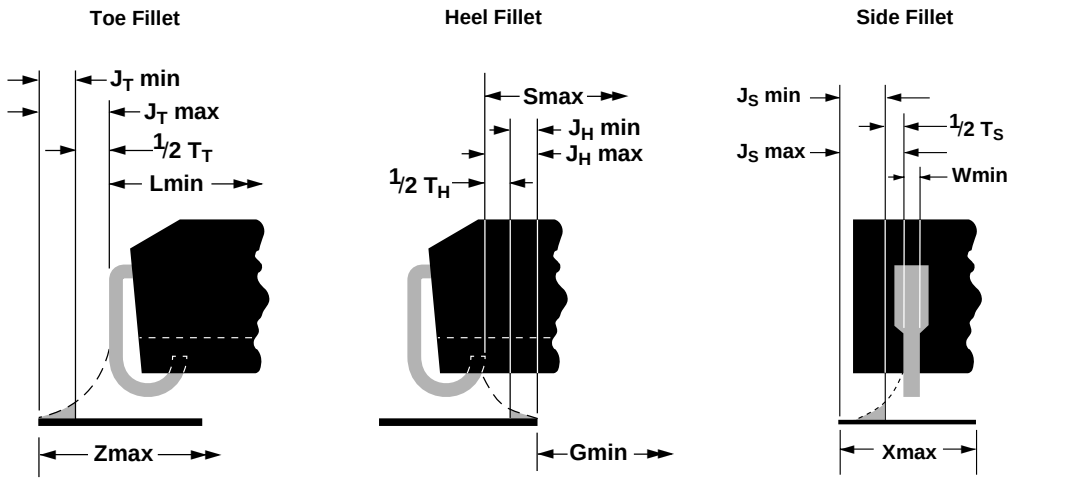
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + $2J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - $2J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + $2J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Heel (mm)			Toe (mm)			Side (mm)		
RLP No.	F	P	C_S	$J_H$min	$J_H$max	C_L	$J_T$min	$J_T$max	C_W	$J_S$min	$J_S$max
480-487A	0.10	0.10	0.38	0.31	0.51	0.68	-0.32	0.03	0.13	-0.01	0.11
490-497A	0.10	0.10	0.38	0.27	0.48	0.68	-0.28	0.07	0.13	-0.01	0.11
500-507A	0.10	0.10	0.38	0.24	0.44	0.68	-0.27	0.10	0.13	-0.01	0.11
510-517A	0.10	0.10	0.38	0.30	0.51	0.68	-0.31	0.04	0.13	-0.01	0.11

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**11.0**
Revision	Subject
	Components with Gullwing Leads on Four Sides

1.0 INTRODUCTION

This section covers land patterns for components with gullwing leads on four sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:
MO 108, issue ''A,'' dated 10/90
MO 112, issue ''A,'' dated 8/90
MO 136, issue ''A,'' dated 8/92, now MS-026
MO 143, issue ''A,'' dated 3/93, now MS-029

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404 General Rules for the Preparation of Outline Drawings of Integrated Circuits

2.3 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description The four-sided gull wing family is characterized by gull wing leads on four sides of a square or rectangular package. The family includes both molded plastic and ceramic case styles. The acronyms PQFP, Plastic Quad Flat Pack and CQFP, Ceramic Quad Flat Pack, are also used to describe the family.

There are several lead pitches within the family from 1.0 mm to 0.30 mm. High lead-count packages are available in this family that accommodate complex, high lead-count chips.

3.2 Marking The PFQP and CQFP families of parts are generally marked with manufacturers part numbers, manufacturers name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/ manufacturing lot and/or manufacturing location.

3.3 Carrier Package Format Components may be provided in tube but packaging tray carriers are preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity required for placement and soldering.

3.3 Process Considerations PQFP and CQFP packages are normally processed by solder reflow operations.

High lead-count fine pitch parts may require special processing outside the normal pick/place and reflow manufacturing operations.

Separate pick/place, excise, and reflow processes are sometimes used as an alternate to normal SMT processes.

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2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for PQFP (Plastic Quad Flat Pack) components. Basic construction of the PQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 and the following for documents applicable to the subsections.

Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Low Profile Plastic Quad Flat Pack Family 0.025 Lead Spacing (Gullwing), Outline MO-086, issue ''B,'' dated 6/90

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3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

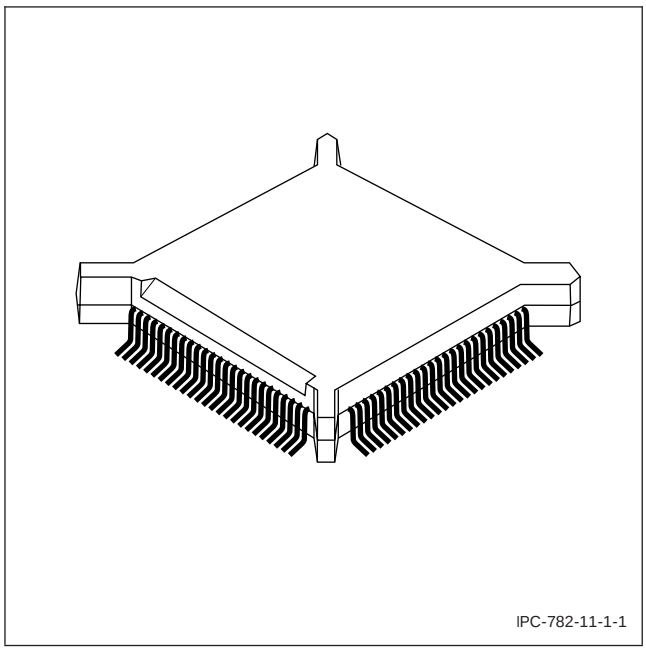


Figure 1 PQFP construction

3.1 Basic Construction See Figure 1. PQFPs have leads on a 0.635 mm pitch.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

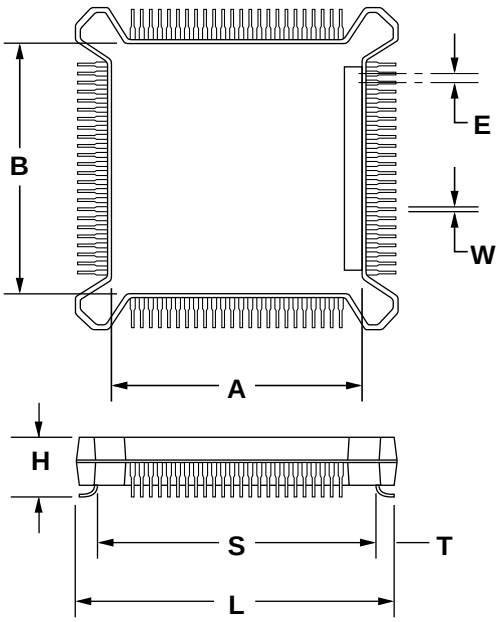
3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for PFQPs is the tube format; however, packaging trays provide the best handling capability.

3.1.4 Process Considerations PQFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PQFP components.



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PQFP Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	E (mm)	H (mm)
	min	max	min	max	min	max	min	max	max	max	basic	max
PQFP 84	19.55	20.05	17.55	18.16	0.20	0.30	0.75	1.00	16.80	16.80	0.635	4.57
PQFP 100	22.10	22.60	20.10	20.71	0.20	0.30	0.75	1.00	19.35	19.35	0.635	4.57
PQFP 132	27.20	27.70	25.25	25.81	0.20	0.30	0.75	1.00	24.40	24.40	0.635	4.57
PQFP 164	32.25	32.75	30.25	30.86	0.20	0.30	0.75	1.00	29.40	29.40	0.635	4.75
PQFP 196	37.35	37.85	35.35	35.96	0.20	0.30	0.75	1.00	34.40	34.40	0.635	4.57
PQFP 244	41.65	42.15	39.65	40.26	0.20	0.30	0.75	1.00	45.40	45.40	0.635	4.57

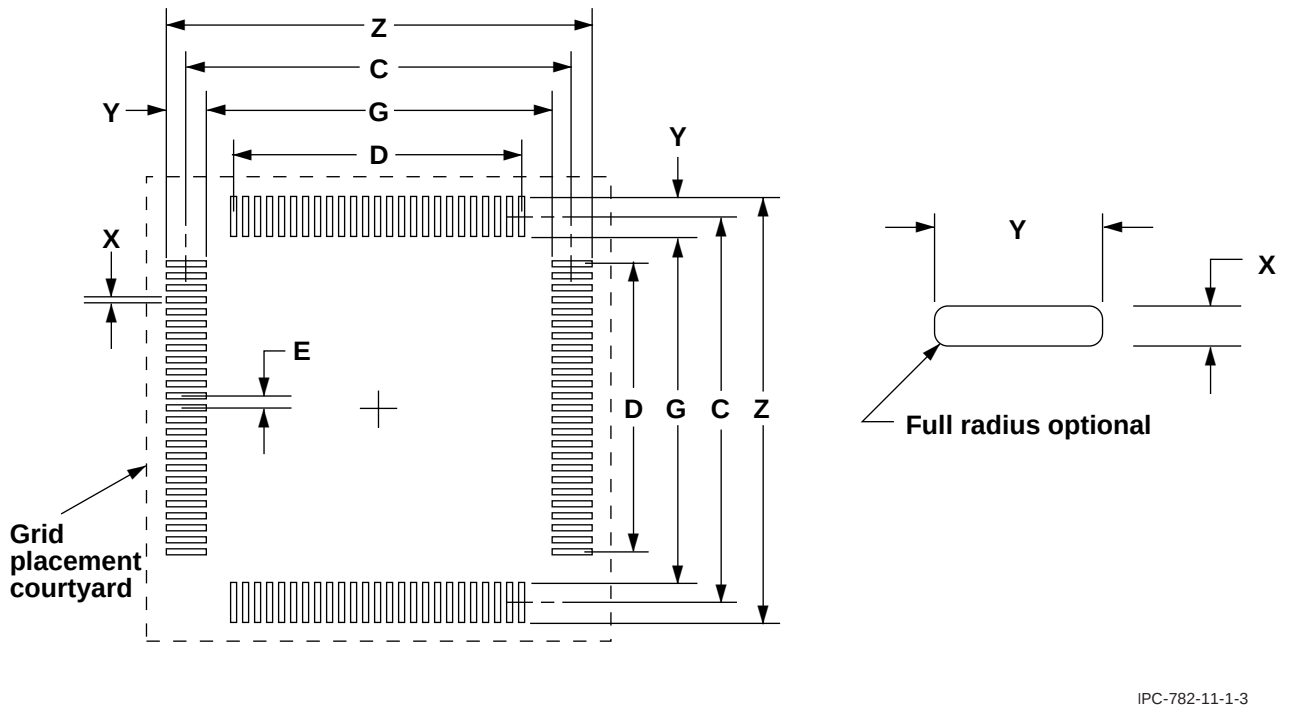
Figure 2 PQFP dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PQFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. of Grid Elements)
530A	PQFP 84	20.60	17.00	0.35	1.80	18.80	12.70	0.63	44X44
531A	PQFP 100	23.20	19.60	0.35	1.80	21.40	15.24	0.63	50X50
532A	PQFP 132	28.20	24.60	0.35	1.80	26.40	20.32	0.63	58X58
533A	PQFP 164	33.40	29.80	0.35	1.80	31.60	25.40	0.63	68X68
534A	PQFP 196	38.40	34.80	0.35	1.80	36.60	30.48	0.63	80X80
535A	PQFP 244	42.80	39.20	0.35	1.80	41.00	38.10	0.63	88X88

Figure 3

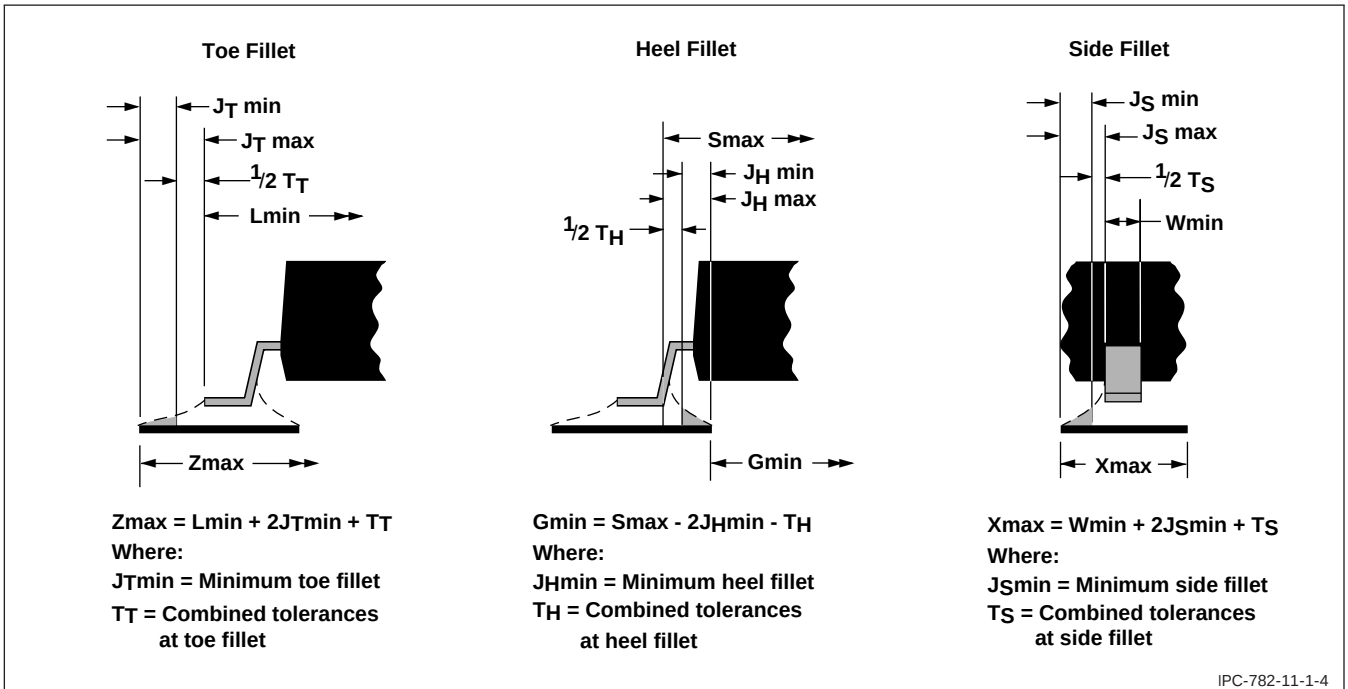
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2JTmin + TT
Where:
JTmin = Minimum toe fillet
TT = Combined tolerances at toe fillet

Gmin = Smax - 2JHmin - TH
Where:
JHmin = Minimum heel fillet
TH = Combined tolerances at heel fillet

Xmax = Wmin + 2JSmin + TS
Where:
JSmin = Minimum side fillet
TS = Combined tolerances at side fillet

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	Tolerance Asssumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
530A	0.10	0.10	0.50	0.27	0.53	0.61	0.27	0.58	0.10	-0.01	0.08
531A	0.10	0.10	0.50	0.29	0.55	0.61	0.24	0.56	0.10	-0.01	0.08
532A	0.10	0.10	0.50	0.24	0.50	0.61	0.29	0.61	0.10	-0.01	0.08
533A	0.10	0.10	0.50	0.32	0.58	0.61	0.22	0.53	0.10	-0.01	0.08
534A	0.10	0.10	0.50	0.27	0.53	0.61	0.27	0.58	0.10	-0.01	0.08
535A	0.10	0.10	0.50	0.32	0.57	0.61	0.22	0.53	0.10	-0.01	0.08

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for square SQFP (Shrink Quad Flat Pack) and QFP (metric plastic quad flat pack) components. Basic construction of the SQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Metric Quad Flat Pack Family 3.2 mm Footprint,'' Outline MO-108, issue ''A,'' dated 10/90

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2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404-1 General Rules for the Preparation of Outline Drawings of Integrated Circuits Fine Pitch Quad Flat Packages (dated January 26, 1989)

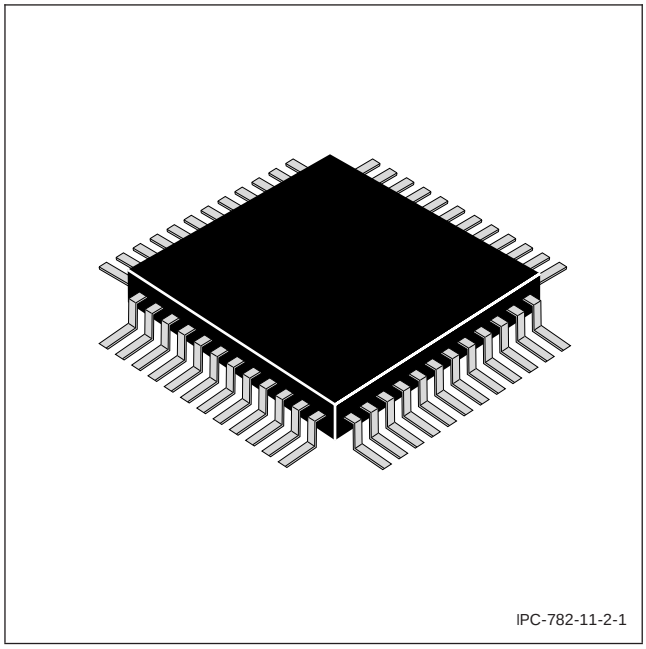


Figure 1 SQFP & QFP (Square)

3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

3.1 Basic Construction See Figure 1.

The shrink quad flat pack has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP family comes in 13 standard sizes, each of which sizes can come in either a 0.5, 0.4, or 0.3 mm pitch. There are therefore 39 configurations for square SQFPs.

Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

QFPs are also square and come in larger pitches. Wherever applicable, the body sizes of the components identified in Figures 2 and 3 show the relationships and pin numbers for SQFPs and QFPs that have the same body size.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

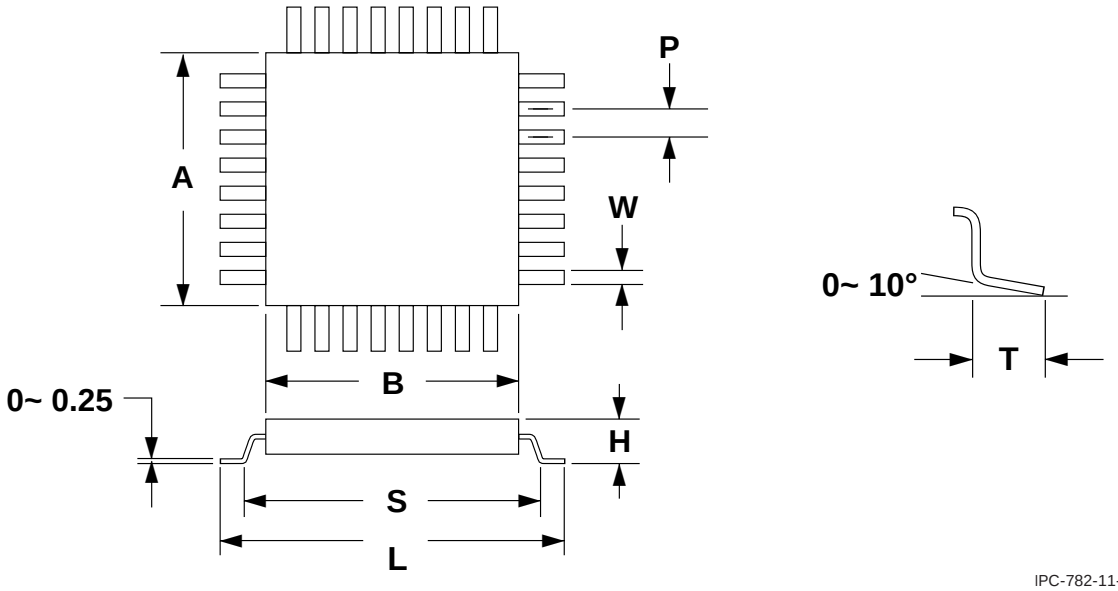
3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for flatpacks may be tube format; but, in most instances, flatpacks are delivered in a carrier tray.

3.1.4 Process Considerations SQFPs and QFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure and 215°C.

4.0 COMPONENT DIMENSIONS

In this subsection, Figures 2a–2d provide the component dimensions for SQFP (Square) components. (Also see pages 4, 6 and 8.)



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
SQFP 5X5-24	6.80	7.20	5.20	5.89	0.10	0.30	0.40	0.80	5.00	5.00	0.50	1.70
SQFP 5X5-32	6.80	7.20	5.20	5.89	0.10	0.30	0.40	0.80	5.00	5.00	0.50	1.70
SQFP 5X5-32-F	6.80	7.20	5.20	5.89	0.05	0.22	0.40	0.80	5.00	5.00	0.40	1.70
SQFP 5X5-40	6.80	7.20	5.20	5.89	0.05	0.22	0.40	0.80	5.00	5.00	0.40	1.70
SQFP 5X5-48	6.80	7.20	5.20	5.89	0.05	0.15	0.40	0.80	5.00	5.00	0.30	1.70
SQFP 5X5-56	6.80	7.20	5.20	5.89	0.05	0.15	0.40	0.80	5.00	5.00	0.30	1.70
SQFP 6X6-32	7.80	8.20	6.20	6.89	0.10	0.30	0.40	0.80	6.00	6.00	0.50	1.70
SQFP 6X6-40	7.80	8.20	6.20	6.89	0.10	0.30	0.40	0.80	6.00	6.00	0.50	1.70
SQFP 6X6-40-F	7.80	8.20	6.20	6.89	0.05	0.22	0.40	0.80	6.00	6.00	0.40	1.70
SQFP 6X6-48	7.80	8.20	6.20	6.89	0.05	0.22	0.40	0.80	6.00	6.00	0.40	1.70
SQFP 6X6-56	7.80	8.20	6.20	6.89	0.05	0.15	0.40	0.80	6.00	6.00	0.30	1.70
SQFP 6X6-64	7.80	8.20	6.20	6.89	0.05	0.15	0.40	0.80	6.00	6.00	0.30	1.70
SQFP 7X7-40	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	7.00	7.00	0.50	1.70
SQFP 7X7-48	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	7.00	7.00	0.50	1.70
SQFP 7X7-56	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	7.00	7.00	0.40	1.70
SQFP 7X7-64	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	7.00	7.00	0.40	1.70
SQFP 7X7-72	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	7.00	7.00	0.30	1.70
SQFP 7X7-80	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	7.00	7.00	0.30	1.70

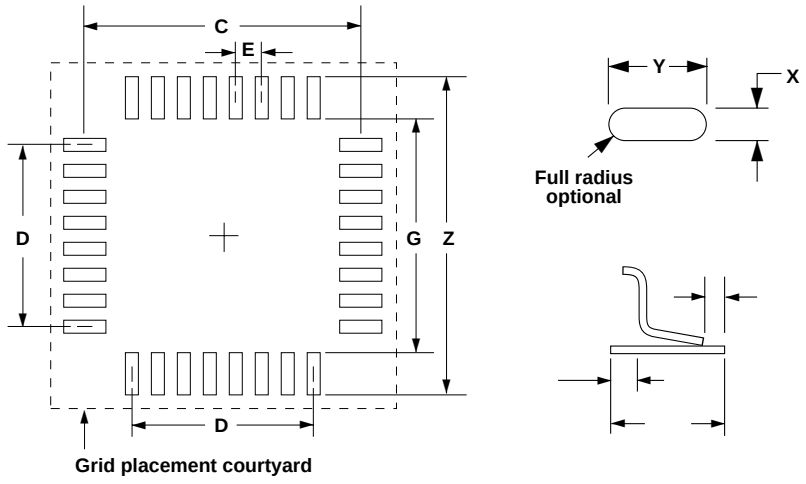
Figure 2a SQFP (Square) component dimensions

5.0 LAND PATTERN DIMENSIONS

In this subsection, Figures 3a–3d provide the land pattern dimensions for SQFP (Square) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns. (Also see pages 5, 7, and 9.)

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 10. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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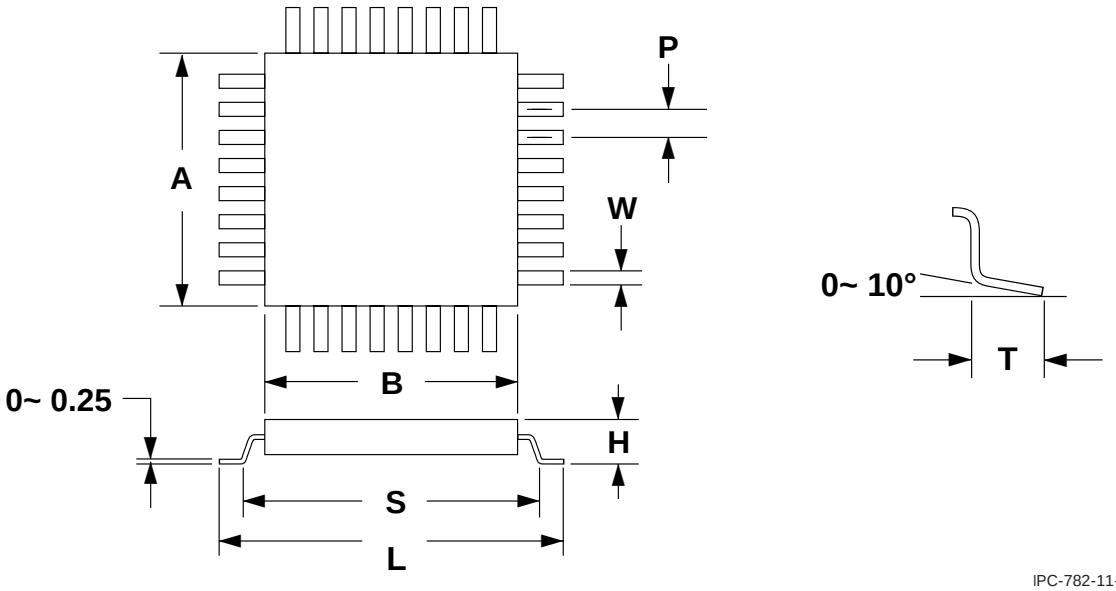
RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
550A	SQFP 5x5-24	7.80	4.60	0.30	1.60	6.20	2.50	0.50	18x18
551A	SQFP 5x5-32	7.80	4.60	0.30	1.60	6.20	3.50	0.50	18x18
552A	SQFP 5x5-32-F	7.80	4.60	0.25	1.60	6.20	2.80	0.40	18x18
553A	SQFP 5x5-40	7.80	4.60	0.25	1.60	6.20	3.60	0.40	18x18
554A	SQFP 5x5-48	7.80	4.60	0.17	1.60	6.20	3.30	0.30	18x18
555A	SQFP 5x5-56	7.80	4.60	0.17	1.60	6.20	3.90	0.30	18x18
556A	SQFP 6x6-32	8.80	5.60	0.30	1.60	7.20	3.50	0.50	20x20
557A	SQFP 6x6-40	8.80	5.60	0.30	1.60	7.20	4.50	0.50	20x20
558A	SQFP 6x6-40-F	8.80	5.60	0.25	1.60	7.20	3.60	0.40	20x20
559A	SQFP 6x6-48	8.80	5.60	0.25	1.60	7.20	4.40	0.40	20x20
560A	SQFP 6x6-56	8.80	5.60	0.17	1.60	7.20	3.90	0.30	20x20
561A	SQFP 6x6-64	8.80	5.60	0.17	1.60	7.20	4.50	0.30	20x20
562A	SQFP 7x7-40	9.80	6.60	0.30	1.60	8.20	4.50	0.50	22x22
563A	SQFP 7x7-48	9.80	6.60	0.30	1.60	8.20	5.50	0.50	22x22
564A	SQFP 7x7-56	9.80	6.60	0.25	1.60	8.20	5.20	0.40	22x22
565A	SQFP 7x7-64	9.80	6.60	0.25	1.60	8.20	6.00	0.40	22x22
566A	SQFP 7x7-72	9.80	6.60	0.17	1.60	8.20	5.10	0.30	22x22
567A	SQFP 7x7-80	9.80	6.60	0.17	1.60	8.20	5.70	0.30	22x22

Figure 3a SQFP (Square) land pattern dimensions



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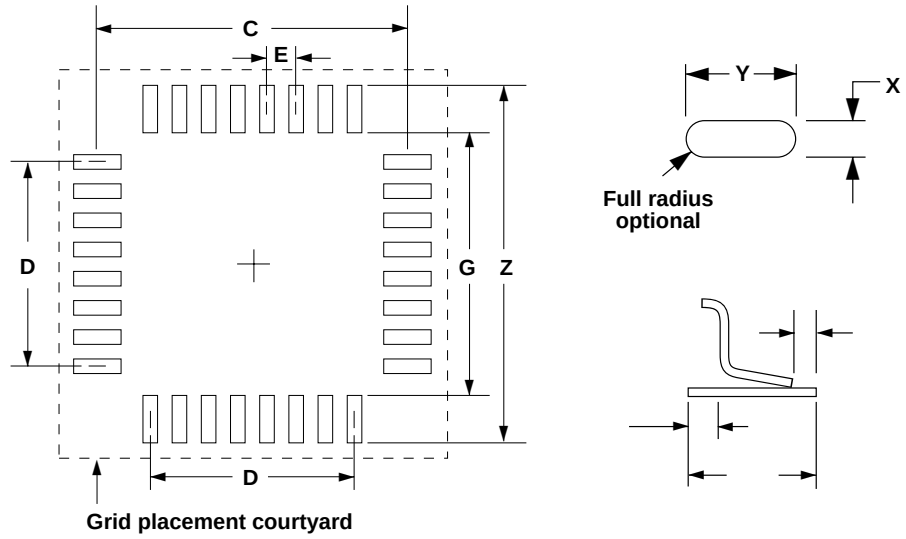
Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
QFP 10x10-44	12.95	13.45	11.05	11.71	0.30	0.45	0.65	0.95	10.00	10.00	0.80	2.45
QFP 10x10-52	12.95	13.45	11.05	11.71	0.22	0.38	0.65	0.95	10.00	10.00	0.65	2.45
SQFP 10x10-64	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	10.00	10.00	0.50	2.20
SQFP 10x10-72	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	10.00	10.00	0.50	2.20
SQFP 10x10-80	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	10.00	10.00	0.40	2.20
SQFP 10x10-88	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	10.00	10.00	0.40	2.20
SQFP 10x10-112	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	10.00	10.00	0.30	2.20
SQFP 10x10-120	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	10.00	10.00	0.30	2.20
QFP 12x12-48	15.00	15.50	13.05	13.71	0.30	0.45	0.65	0.95	12.00	12.00	0.80	2.45
QFP 12x12-64	15.00	15.50	13.05	13.71	0.22	0.38	0.65	0.95	12.00	12.00	0.65	2.45
SQFP 12x12-80	13.80	14.20	12.20	12.89	0.10	0.30	0.40	0.80	12.00	12.00	0.50	2.20
SQFP 12x12-88	13.80	14.20	12.20	12.89	0.10	0.30	0.40	0.80	12.00	12.00	0.50	2.20
SQFP 12x12-100	13.80	14.20	12.20	12.89	0.05	0.22	0.40	0.80	12.00	12.00	0.40	2.20
SQFP 12x12-108	13.80	14.20	12.20	12.89	0.05	0.22	0.40	0.80	12.00	12.00	0.40	2.20
SQFP 12x12-136	13.80	14.20	12.20	12.89	0.05	0.15	0.40	0.80	12.00	12.00	0.30	2.20
SQFP 12x12-144	13.80	14.20	12.20	12.89	0.05	0.15	0.40	0.80	12.00	12.00	0.30	2.20
QFP 14x14-64	16.95	17.45	15.05	15.71	0.30	0.45	0.65	0.95	14.00	14.00	0.80	2.45
QFP 14x14-80	16.95	17.45	15.05	15.71	0.22	0.38	0.65	0.95	14.00	14.00	0.65	2.45
SQFP 14x14-100	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	14.00	14.00	0.50	2.20
SQFP 14x14-108	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	14.00	14.00	0.50	2.20
SQFP 14x14-120	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	14.00	14.00	0.40	2.20
SQFP 14x14-128	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	14.00	14.00	0.40	2.20
SQFP 14x14-168	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	14.00	14.00	0.30	2.20
SQFP 14x14-176	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	14.00	14.00	0.30	2.20

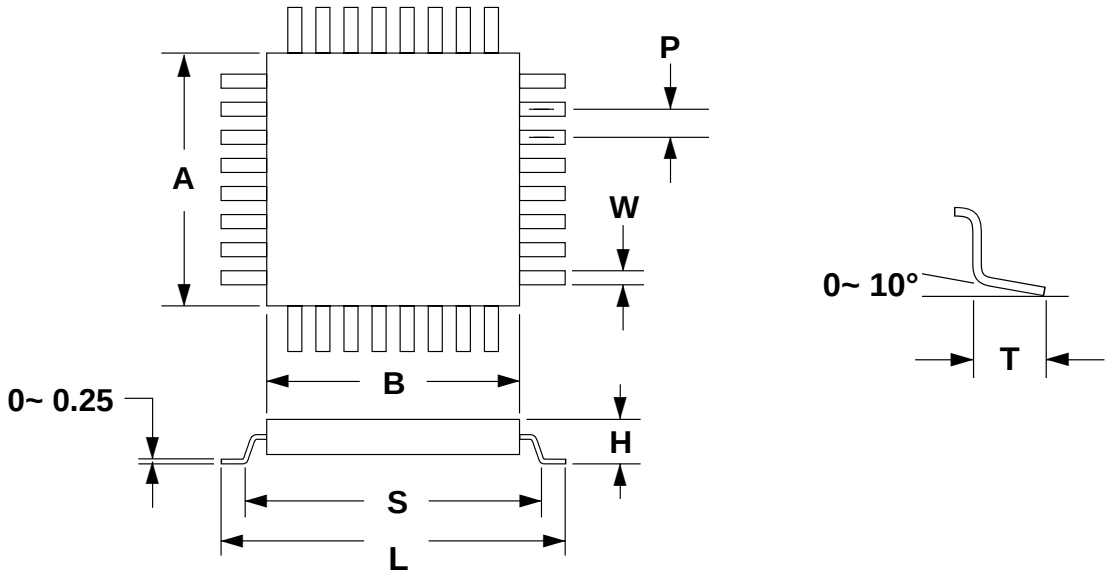
Figure 2b SQFP/QFP (square) component dimensions



IPC-782-11-2-3b

RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) basic	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
570A	QFP 10x10-44	13.80	10.20	0.50	1.80	12.00	8.00	0.80	30x30
571A	QFP 10x10-52	13.80	10.20	0.40	1.80	12.00	7.80	0.65	30x30
572A	SQFP 10x10-64	12.80	9.60	0.30	1.60	11.20	7.50	0.50	28x28
573A	SQFP 10x10-72	12.80	9.60	0.30	1.60	11.20	8.50	0.50	28x28
574A	SQFP 10x10-80	12.80	9.60	0.25	1.60	11.20	7.60	0.40	28x28
575A	SQFP 10x10-88	12.80	9.60	0.25	1.60	11.20	8.40	0.40	28x28
576A	SQFP 10x10-112	12.80	9.60	0.17	1.60	11.20	8.10	0.30	28x28
577A	SQFP 10x10-120	12.80	9.60	0.17	1.60	11.20	8.70	0.30	28x28
580A	QFP 12x12-48	16.00	12.40	0.50	1.80	14.20	8.80	0.80	34x34
581A	QFP 12x12-64	16.00	12.40	0.40	1.80	14.20	9.75	0.65	34x34
582A	SQFP 12x12-80	14.80	11.60	0.30	1.60	13.20	9.50	0.50	32x32
583A	SQFP 12x12-88	14.80	11.60	0.30	1.60	13.20	10.50	0.50	32x32
584A	SQFP 12x12-100	14.80	11.60	0.25	1.60	13.20	9.60	0.40	32x32
585A	SQFP 12x12-108	14.80	11.60	0.25	1.60	13.20	10.40	0.40	32x32
586A	SQFP 12x12-136	14.80	11.60	0.17	1.60	13.20	9.90	0.30	32x32
587A	SQFP 12x12-144	14.80	11.60	0.17	1.60	13.20	10.50	0.30	32x32
590A	QFP 14x14-64	17.80	14.20	0.50	1.80	16.00	12.00	0.80	38x38
591A	QFP 14x14-80	17.80	14.20	0.40	1.80	16.00	12.35	0.65	38x38
592A	SQFP 14x14-100	16.80	13.60	0.30	1.60	15.20	12.00	0.50	36x36
593A	SQFP 14x14-108	16.80	13.60	0.30	1.60	15.20	13.00	0.50	36x36
594A	SQFP 14x14-120	16.80	13.60	0.25	1.60	15.20	11.60	0.40	36x36
595A	SQFP 14x14-128	16.80	13.60	0.25	1.60	15.20	12.40	0.40	36x36
596A	SQFP 14x14-168	16.80	13.60	0.17	1.60	15.20	12.30	0.30	36x36
597A	SQFP 14x14-176	16.80	13.60	0.17	1.60	15.20	12.90	0.30	36x36

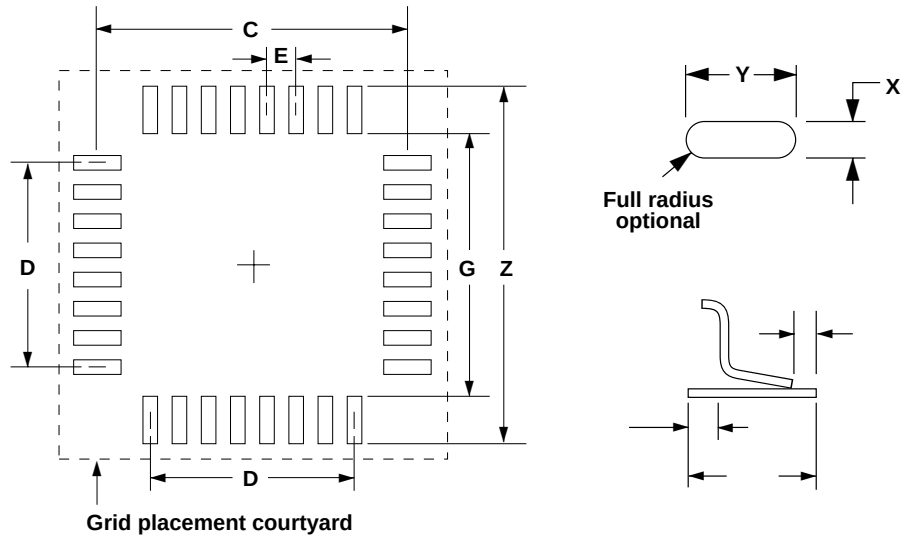
Figure 3b SQFP/QFP (square) land pattern dimensions



IPC-782-11-2-2b

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
SQFP 20x20-144	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	20.00	20.00	0.50	2.70
SQFP 20x20-152	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	20.00	20.00	0.50	2.70
SQFP 20x20-184	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	20.00	20.00	0.40	2.70
SQFP 20x20-192	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	20.00	20.00	0.40	2.70
SQFP 20x20-248	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	20.00	20.00	0.30	2.70
SQFP 20x20-256	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	20.00	20.00	0.30	2.70
SQFP 24x24-176	25.80	26.20	24.20	24.89	0.10	0.30	0.40	0.80	24.00	24.00	0.50	3.20
SQFP 24x24-184	25.80	26.20	24.20	24.89	0.10	0.30	0.40	0.80	24.00	24.00	0.50	3.20
SQFP 24x24-224	25.80	26.20	24.20	24.89	0.05	0.22	0.40	0.80	24.00	24.00	0.40	3.20
SQFP 24x24-232	25.80	26.20	24.20	24.89	0.05	0.22	0.40	0.80	24.00	24.00	0.40	3.20
SQFP 24x24-296	25.80	26.20	24.20	24.89	0.05	0.15	0.40	0.80	24.00	24.00	0.30	3.20
SQFP 24x24-304	25.80	26.20	24.20	24.89	0.05	0.15	0.40	0.80	24.00	24.00	0.30	3.20
QFP 28x28-120	30.95	31.45	29.05	29.71	0.30	0.45	0.65	0.95	28.00	28.00	0.80	3.75
QFP 28x28-128	30.95	31.45	29.05	29.71	0.30	0.45	0.65	0.95	28.00	28.00	0.80	3.75
QFP 28x28-144	30.95	31.45	29.05	29.71	0.22	0.38	0.65	0.95	28.00	28.00	0.65	3.75
QFP 28x28-160	30.95	31.45	29.05	29.71	0.22	0.38	0.65	0.95	28.00	28.00	0.65	3.75
SQFP 28x28-208	29.80	30.60	28.20	28.89	0.10	0.30	0.40	0.80	28.00	28.00	0.50	3.75
SQFP 28x28-216	29.80	30.60	28.20	28.89	0.10	0.30	0.40	0.80	28.00	28.00	0.50	3.75
SQFP 28x28-264	29.80	30.60	28.20	28.89	0.05	0.22	0.40	0.80	28.00	28.00	0.40	3.75
SQFP 28x28-272	29.80	30.60	28.20	28.89	0.05	0.22	0.40	0.80	28.00	28.00	0.40	3.75
SQFP 28x28-352	29.80	30.60	28.20	28.89	0.05	0.15	0.40	0.80	28.00	28.00	0.30	3.75
SQFP 28x28-360	29.80	30.60	28.20	28.89	0.05	0.15	0.40	0.80	28.00	28.00	0.30	3.75

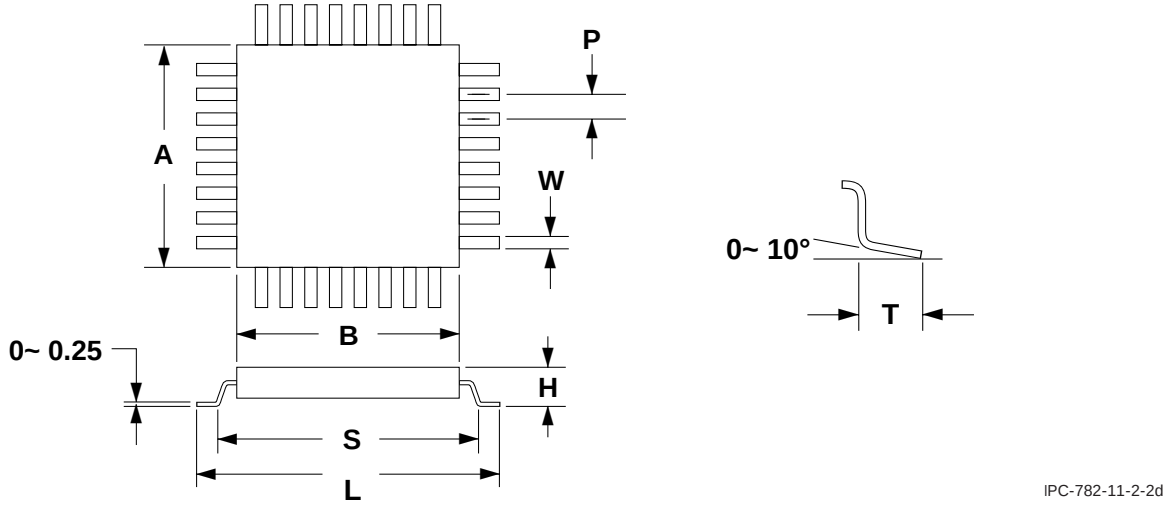
Figure 2c SQFP/QFP (square) component dimensions



IPC-782-11-2-3c

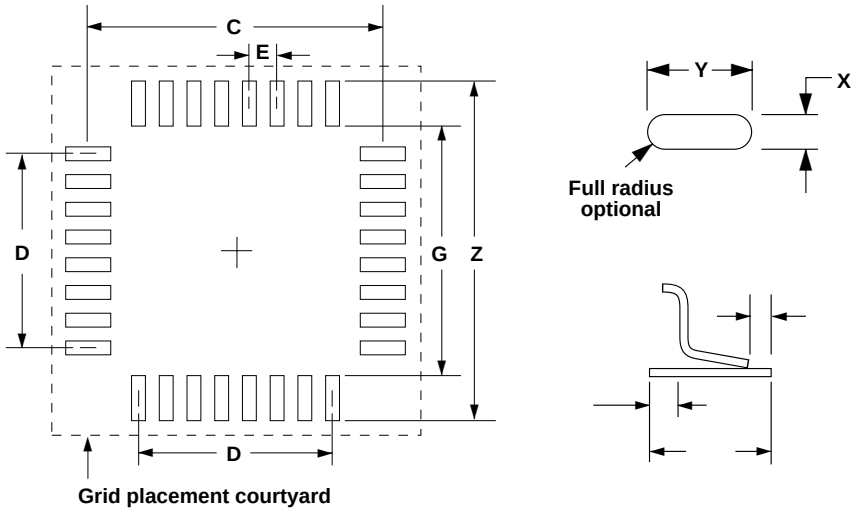
RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
600A	SQFP 20x20-144	22.80	19.60	0.30	1.60	21.20	17.50	0.50	48x48
601A	SQFP 20x20-152	22.80	19.60	0.30	1.60	21.20	18.50	0.50	48x48
602A	SQFP 20x20-184	22.80	19.60	025	1.60	21.20	18.00	0.40	48x48
603A	SQFP 20x20-192	22.80	19.60	0.25	1.60	21.20	18.80	0.40	48x48
604A	SQFP 20x20-248	22.80	19.60	0.17	1.60	21.20	18.30	0.30	48x48
605A	SQFP 20x20-256	22.80	19.60	0.17	1.60	21.20	18.90	0.30	48x48
609A	SQFP 24x24-176	26.80	23.60	0.30	1.60	25.20	21.50	0.50	56x56
610A	SQFP 24x24-184	26.80	23.60	0.30	1.60	25.20	22.50	0.50	56x56
611A	SQFP 24x24-224	26.80	23.60	0.25	1.60	25.20	22.00	0.40	56x56
612A	SQFP 24x24-232	26.80	23.60	0.25	1.60	25.20	22.80	0.40	56x56
613A	SQFP 24x24-296	26.80	23.60	0.17	1.60	25.20	21.90	0.30	56x56
614A	SQFP 24x24-304	26.80	23.60	0.17	1.60	25.20	22.50	0.30	56x56
618A	QFP 28x28-120	31.80	28.20	0.50	1.80	30.00	23.20	0.80	66x66
619A	QFP 28x28-128	31.80	28.20	0.50	1.80	30.00	24.80	0.80	66x66
620A	QFP 28x28-144	31.80	28.20	0.40	1.80	30.00	22.75	0.65	66x66
621A	QFP 28x28-160	31.80	28.20	0.40	1.80	30.00	25.35	0.65	66x66
622A	SQFP 28x28-208	30.80	27.60	0.30	1.60	29.20	25.50	0.50	64x64
623A	SQFP 28x28-216	30.80	27.60	0.30	1.60	29.20	26.50	0.50	64x64
624A	SQFP 28x28-264	30.80	27.60	0.25	1.60	29.20	26.00	0.40	64x64
625A	SQFP 28x28-272	30.80	27.60	0.25	1.60	29.20	26.80	0.40	64x64
626A	SQFP 28x28-352	30.80	27.60	0.17	1.60	29.20	26.10	0.30	64x64
627A	SQFP 28x28-360	30.80	27.60	0.17	1.60	29.20	26.70	0.30	64x64

Figure 3c SQFP/QFP (square) land pattern dimensions



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
QFP 32x32-184	34.95	35.45	33.05	33.71	0.22	0.38	0.65	0.95	32.00	32.00	0.65	4.20
SQFP 32x32-240	33.80	34.20	32.20	32.89	0.10	0.30	0.40	0.80	32.00	32.00	0.50	4.20
SQFP 32x32-248	33.80	34.20	32.20	32.89	0.10	0.30	0.40	0.80	32.00	32.00	0.50	4.20
SQFP 32x32-304	33.80	34.20	32.20	32.89	0.05	0.22	0.40	0.80	32.00	32.00	0.40	4.20
SQFP 32x32-312	33.80	34.20	32.20	32.89	0.05	0.22	0.40	0.80	32.00	32.00	0.40	4.20
SQFP 32x32-400	33.80	34.20	32.20	32.89	0.05	0.15	0.40	0.80	32.00	32.00	0.30	4.20
SQFP 32x32-408	33.80	34.20	32.20	32.89	0.05	0.15	0.40	0.80	32.00	32.00	0.30	4.20
SQFP 36x36-272	37.80	38.20	36.20	36.89	0.10	0.30	0.40	0.80	36.00	36.00	0.50	4.20
SQFP 36x36-280	37.80	38.20	36.20	36.89	0.10	0.30	0.40	0.80	36.00	36.00	0.50	4.20
SQFP 36x36-344	37.80	38.20	36.20	36.89	0.05	0.22	0.40	0.80	36.00	36.00	0.40	4.20
SQFP 36x36-352	37.80	38.20	36.20	36.89	0.05	0.22	0.40	0.80	36.00	36.00	0.40	4.20
SQFP 36x36-456	37.80	38.20	36.20	36.89	0.05	0.15	0.40	0.80	36.00	36.00	0.30	4.20
SQFP 36x36-464	37.80	38.20	36.20	36.89	0.05	0.15	0.40	0.80	36.00	36.00	0.30	4.20
QFP 40x40-232	42.95	43.45	41.05	41.71	0.22	0.38	0.65	0.95	40.00	40.00	0.65	4.20
SQFP 40x40-304	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	40.00	40.00	0.50	4.20
SQFP 40x40-312	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	40.00	40.00	0.50	4.20
SQFP 40x40-384	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	40.00	40.00	0.40	4.20
SQFP 40x40-392	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	40.00	40.00	0.40	4.20
SQFP 40x40-512	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	40.00	40.00	0.30	4.20
SQFP 40x40-520	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	40.00	40.00	0.30	4.20
SQFP 44x44-336	45.80	46.20	44.20	44.89	0.10	0.30	0.40	0.80	44.00	44.00	0.50	4.20
SQFP 44x44-344	45.80	46.20	44.20	44.89	0.10	0.30	0.40	0.80	44.00	44.00	0.50	4.20
SQFP 44x44-424	45.80	46.20	44.20	44.89	0.05	0.22	0.40	0.80	44.00	44.00	0.40	4.20
SQFP 44x44-432	45.80	46.20	44.20	44.89	0.05	0.22	0.40	0.80	44.00	44.00	0.40	4.20
SQFP 44x44-568	45.80	46.20	44.20	44.89	0.05	0.15	0.40	0.80	44.00	44.00	0.30	4.20
SQFP 44x44- 576	45.80	46.20	44.20	44.89	0.05	0.15	0.40	0.80	44.00	44.00	0.30	4.20

Figure 2d SQFP/QFP (square) component dimensions



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
630A	QFP 32x32-184	35.80	32.20	0.40	1.80	34.00	29.25	0.65	74x74
631A	SQFP 32x32-240	34.80	31.60	0.30	1.60	33.20	29.50	0.50	72x72
632A	SQFP 32x32-248	34.80	31.60	0.30	1.60	33.20	30.50	0.50	72x72
633A	SQFP 32x32-304	34.80	31.60	0.25	1.60	33.20	30.00	0.40	72x72
634A	SQFP 32x32-312	34.80	31.60	0.25	1.60	33.20	30.80	0.40	72x72
635A	SQFP 32x32-400	34.80	31.60	0.17	1.60	33.20	29.70	0.30	72x72
636A	SQFP 32x32-408	34.80	35.60	0.17	1.60	33.20	30.30	0.30	72x72
640A	SQFP 36x36-272	38.80	35.60	0.30	1.60	37.20	33.50	0.50	80x80
641A	SQFP 36x36-280	38.80	35.60	0.30	1.60	37.20	34.50	0.50	80x80
642A	SQFP 36x36-344	38.80	35.60	0.25	1.60	37.20	34.00	0.40	80x80
643A	SQFP 36x36-352	38.80	35.60	0.25	1.60	37.20	34.80	0.40	80x80
644A	SQFP 36x36-456	38.80	35.60	0.17	1.60	37.20	33.90	0.30	80x80
645A	SQFP 36x36-464	38.80	35.60	0.17	1.60	37.20	34.50	0.30	80x80
650A	QFP 40x40-232	43.80	40.20	0.40	1.80	42.00	37.05	0.65	90x90
651A	SQFP 40x40-304	42.80	39.60	0.30	1.60	41.20	37.50	0.50	88x88
652A	SQFP 40x40-312	42.80	39.60	0.30	1.60	41.20	38.50	0.50	88x88
653A	SQFP 40x40-384	42.80	39.60	0.25	1.60	41.20	38.00	0.40	88x88
654A	SQFP 40x40-392	42.80	39.60	0.25	1.60	41.20	38.80	0.40	88x88
655A	SQFP 40x40-512	42.80	39.60	0.17	1.60	41.20	38.10	0.30	88x88
656A	SQFP 40x40-520	42.80	39.60	0.17	1.60	41.20	38.70	0.30	88x88
660A	SQFP 44x44-336	46.80	43.60	0.30	1.60	45.20	41.50	0.50	96x96
661A	SQFP 44x44-344	46.80	43.60	0.30	1.60	45.20	42.50	0.50	96x96
662A	SQFP 44x44-424	46.80	43.60	0.25	1.60	45.20	42.00	0.40	96x96
663A	SQFP 44x44-432	46.80	43.60	0.25	1.60	45.20	42.80	0.40	96x96
664A	SQFP 44x44-568	46.80	43.60	0.17	1.60	45.20	42.30	0.30	96x96
665A	SQFP 44x44-576	46.80	43.60	0.17	1.60	45.20	42.90	0.30	96x96

Figure 3d SQFP/QFP (square) land pattern dimensions

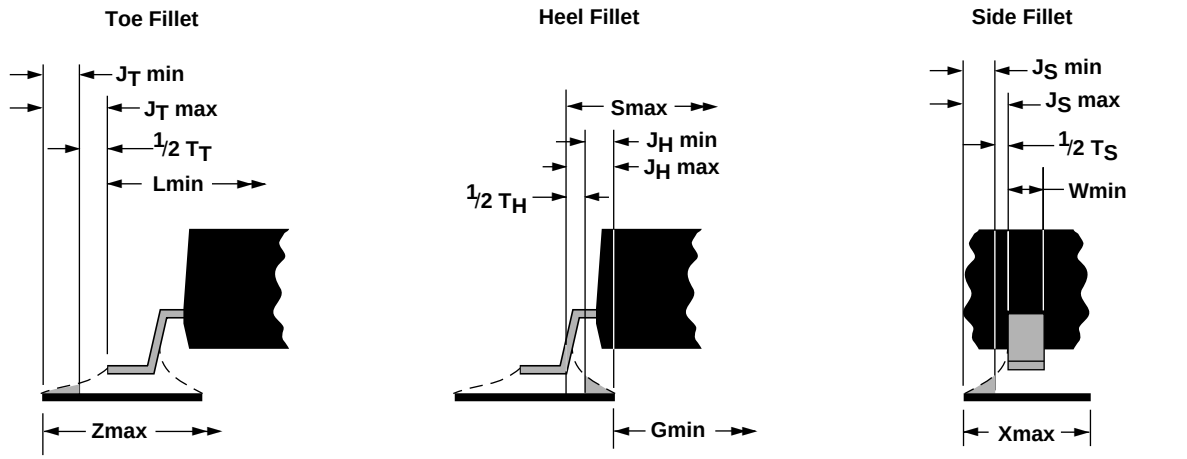
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2$J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - 2$J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + 2$J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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Component Pitch (mm)	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
Basic	F	P	C_L	J_T min	$J_T$max	C_S	$J_H$min	$J_H$max	C_w	$J_S$min	$J_S$max
0.80	0.10	0.10	0.50	0.17	0.43	0.66	0.42	0.75	0.15	0.00	0.10
0.65	0.10	0.10	0.50	0.17	0.43	0.66	0.42	0.75	0.16	–0.02	0.09
0.50	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.20	–0.02	0.10
0.40	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.17	–0.01	0.10
0.30	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.10	–0.03	0.06

Figure 4 Tolerance and solder joint analysis

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**11.3**
Revision	Subject
A	**SQFP/QFP (Rectangular)**

1.0 SCOPE

This subsection provides the component and land pattern dimensions for rectangular SQFP (Shrink Quad Flat Pack) and the QFP (metric plastic quad flat pack) components. Basic construction of the SQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 for documents applicable to the subsections.

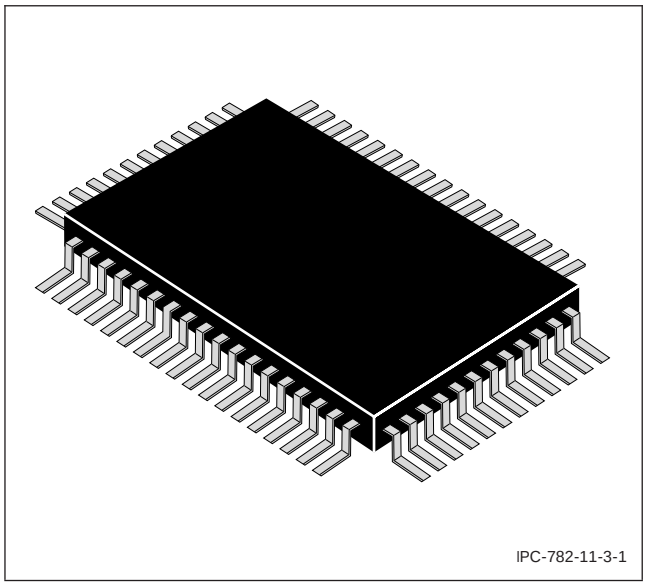
2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Metric Quad Flat Pack Family 3.2 mm Footprint,'' Outline MO-108, issue ''A,'' dated 10/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404-1 General Rules for the Preparation of Outline Drawings of Integrated Circuits Fine Pitch Quad Flat Packages (dated January 26, 1989)



IPC-782-11-3-1

SQFP (Rectangular)

3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

3.1 Basic Construction See Figure 1.

The shrink quad flat pack has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP family comes in 13 standard sizes, each of which sizes can come in either a 0.5, 0.4, or 0.3 mm pitch. There are therefore 39 configurations for square SQFPs.

Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

QFPs are also square and come in larger pitches. Wherever applicable, the body sizes of the components identified in Figures 2 and 3 show the relationships and pin numbers for SQFPs and QFPs that have the same body size.

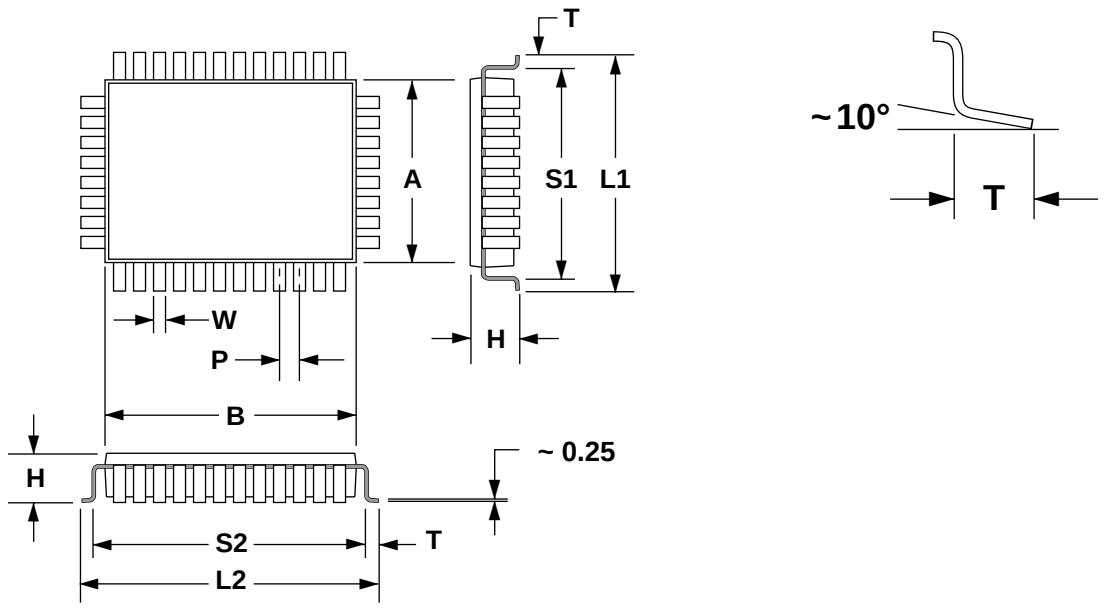
3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for flat packs may be tube format; but, in most instances, flat packs are delivered in a carrier tray.

3.1.4 Process Considerations SQFPs and QFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 Component Dimensions In this subsection, Figures 2a-2b provide the component dimensions for SOJ components. (Also see page 4.)



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Component Identifier	L1 (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		P (mm)	H (mm)	A (mm)	B (mm)	Pin count, short side	Pin count, long side
	min	max	min	max	min	max	min	max	min	max	min	max	basic	max	ref	ref		
SQFP 5X7-32	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	0.50	1.70	5.00	7.00	6	10
SQFP 5X7-40	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	0.50	1.70	5.00	7.00	8	12
SQFP 5X7-44	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	0.40	1.70	5.00	7.00	8	14
SQFP 5X7-52	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	0.40	1.70	5.00	7.00	10	16
SQFP 5X7-60	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	0.30	1.70	5.00	7.00	12	18
SQFP 5X7-68	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	0.30	1.70	7.00	10.00	14	20
SQFP 7X10-52	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	0.50	2.20	7.00	10.00	10	16
SQFP 7X10-60	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	0.50	2.20	7.00	10.00	12	18
SQFP 7X10-68	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	0.40	2.20	7.00	10.00	14	20
SQFP 7X10-76	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	0.40	2.20	7.00	10.00	16	22
SQFP 7X10-92	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	0.30	2.20	7.00	10.00	18	28
SQFP 7X10-100	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	0.30	2.20	7.00	10.00	20	30
SQFP 10X14-80	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	0.50	2.20	10.00	14.00	16	24
SQFP 10X14-88	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	0.50	2.20	10.00	14.00	18	26
SQFP 10X14-100	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	0.40	2.20	10.00	14.00	20	30
SQFP 10X14-108	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	0.40	2.20	10.00	14.00	22	32
SQFP 10X14-140	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	0.30	2.20	10.00	14.00	28	42
SQFP 10X14-148	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	0.30	2.20	10.00	14.00	30	44

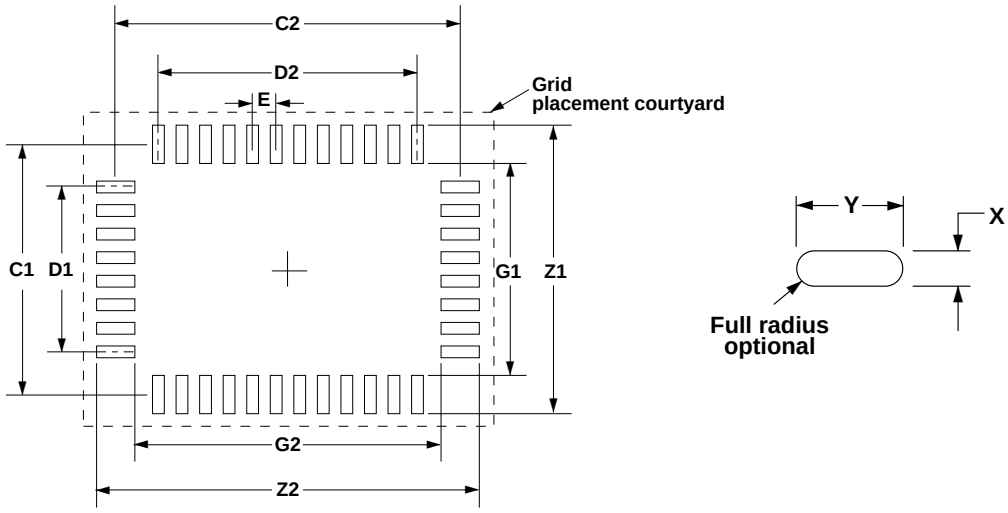
Figure 2a SQFP (Rectangular) component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SQFP (Rectangular) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

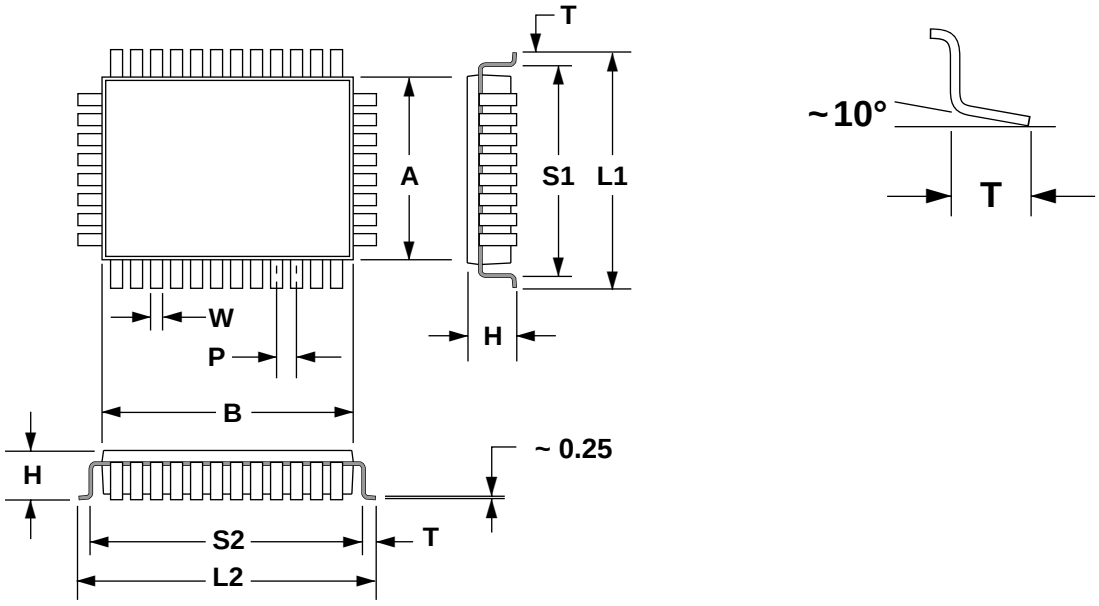
In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 6. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm) ref	C1 (mm) ref	D1 (mm) ref	C2 (mm) ref	D2 (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
680A	SQFP 5x7-32	7.80	4.60	9.80	6.60	0.30	1.60	6.20	2.50	8.20	4.50	0.50	18x22
681A	SQFP 5x7-40	7.80	4.60	9.80	6.60	0.30	1.60	6.20	3.50	8.20	5.50	0.50	18x22
682A	SQFP 5x7-44	7.80	4.60	9.80	6.60	0.25	1.60	6.20	2.80	8.20	5.20	0.40	18x22
683A	SQFP 5x7-52	7.80	4.60	9.80	6.60	0.25	1.60	6.20	3.60	8.20	6.00	0.40	18x22
684A	SQFP 5x7-60	7.80	4.60	9.80	6.60	0.17	1.60	6.20	3.30	8.20	5.10	0.30	18x22
685A	SQFP 5x7-68	7.80	4.60	9.80	6.60	0.17	1.60	6.20	3.90	8.20	5.70	0.30	18x22
690A	SQFP 7x10-52	9.80	6.60	12.80	9.60	0.30	1.60	8.20	4.50	11.20	7.50	0.50	22x28
691A	SQFP 7x10-60	9.80	6.60	12.80	9.60	0.30	1.60	8.20	5.50	11.20	8.50	0.50	22x28
692A	SQFP 7x10-68	9.80	6.60	12.80	9.60	0.25	1.60	8.20	5.20	11.20	7.60	0.40	22x28
693A	SQFP 7x10-76	9.80	6.60	12.80	9.60	0.25	1.60	8.20	6.00	11.20	8.40	0.40	22x28
694A	SQFP 7x10-92	9.80	6.60	12.80	9.60	0.17	1.60	8.20	5.10	11.20	8.10	0.30	22x28
695A	SQFP 7x10-100	9.80	6.60	12.80	9.60	0.17	1.60	8.20	5.70	11.20	8.70	0.30	22x28
700A	SQFP 10x14-80	12.80	9.60	16.80	13.60	0.30	1.60	11.20	7.50	15.20	11.50	0.50	28x36
701A	SQFP 10x14-88	12.80	9.60	16.80	13.60	0.30	1.60	11.20	8.50	15.20	12.50	0.50	28x36
702A	SQFP 10x14-100	12.80	9.60	16.80	13.60	0.25	1.60	11.20	7.60	15.20	11.60	0.40	28x36
703A	SQFP 10x14-108	12.80	9.60	16.80	13.60	0.25	1.60	11.20	8.40	15.20	12.40	0.40	28x36
704A	SQFP 10x14- 140	12.80	9.60	16.80	13.60	0.17	1.60	11.20	8.10	15.20	12.30	0.30	28x36
705A	SQFP 10x14-148	12.80	9.60	16.80	13.60	0.17	1.60	11.20	8.70	15.20	12.90	0.30	28x36

Figure 3a SQFP (Rectangular) land pattern dimensions



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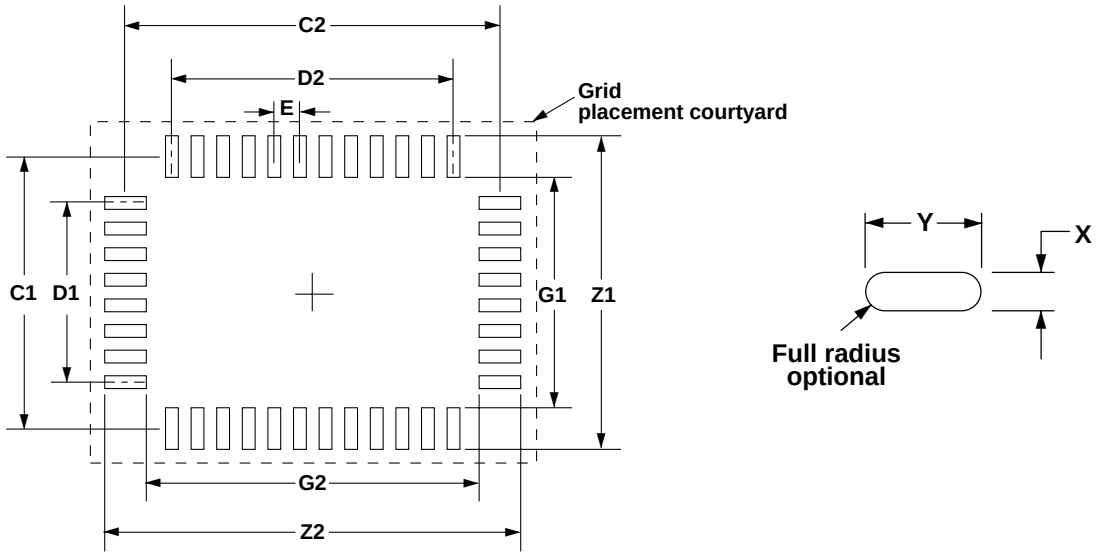
Component Identifier	L (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		P (mm)	H (mm)	A (mm)	B (mm)	Pin Count, Short Side	Pin Count, Long Side
	min	max	min	max	min	max	min	max	min	max	min	max	basic	max	ref	ref		
QFP-14x20-80	16.95	17.45	14.85	15.55	22.95	23.45	20.85	21.55	0.30	0.45	0.70	1.05	0.80	2.45	14.00	20.00	16	24
QFP-14x20-100	16.95	17.45	14.85	15.55	22.95	23.45	20.85	21.55	0.22	0.38	0.70	1.05	0.65	2.45	14.00	20.00	20	30
SQFP-14x20-120	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	0.50	2.20	14.00	20.00	24	36
SQFP-14x20-128	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	0.50	2.20	14.00	20.00	26	38
SQFP-14x20-152	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	0.40	2.20	14.00	20.00	30	46
SQFP-14x20-160	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	0.40	2.20	14.00	20.00	32	48
SQFP-14x20-208	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	0.30	2.20	14.00	20.00	42	62
SQFP-14x20-216	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	0.30	2.20	14.00	20.00	44	64
SQFP-20x28-176	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.10	0.30	0.40	0.80	0.50	3.75	20.00	28.00	36	52
SQFP-20x28-184	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.10	0.30	0.40	0.80	0.50	3.75	20.00	28.00	38	54
SQFP-20x28-224	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.22	0.40	0.80	0.40	3.75	20.00	28.00	46	66
SQFP-20x28-232	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.22	0.40	0.80	0.40	3.75	20.00	28.00	48	68
SQFP-20x28-300	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.15	0.40	0.80	0.30	3.75	20.00	28.00	62	88
SQFP-20x28-308	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.15	0.40	0.80	0.30	3.75	20.00	28.00	64	90
SQFP-28x40-256	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	0.50	4.20	28.00	28.00	52	76
SQFP-28x40-264	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	0.50	4.20	28.00	40.00	54	78
SQFP-28x40-324	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	0.40	4.20	28.00	40.00	66	96
SQFP-28x40-332	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	0.40	4.20	28.00	40.00	68	98
SQFP-28x40-432	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	0.30	4.20	28.00	40.00	88	128
SQFP-28x40-440	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	0.30	4.20	28.00	40.00	90	130

Figure 2b SQFP/QFP (Rectangular) component dimensions



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RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm)	C1 (mm)	D1 (mm)	C2 (mm)	D2 (mm)	E (mm)	Placement Grid (No. of Grid Elements)
							ref	ref	ref	ref	ref	ref	
710A	QFP 14X20-80	18.00	14.40	24.00	20.40	0.50	1.80	16.20	12.00	22.20	18.40	0.80	38x50
711A	QFP 14X20-100	18.00	14.40	24.00	20.40	0.40	1.80	16.20	12.35	22.20	18.85	0.65	38x50
712A	SQFP 14X20-120	16.80	13.60	22.80	19.60	0.30	1.60	15.20	11.50	21.20	17.50	0.50	36x48
713A	SQFP 14X20-128	16.80	13.60	22.80	19.60	0.30	1.60	15.20	12.50	21.20	18.50	0.50	36x48
714A	SQFP 14X20-152	16.80	13.60	22.80	19.60	0.25	1.60	15.20	11.60	21.20	18.00	0.40	36x48
715A	SQFP 14X20-160	16.80	13.60	22.80	19.60	0.25	1.60	15.20	12.40	21.20	18.80	0.40	36x48
716A	SQFP 14X20-208	16.80	13.60	22.80	19.60	0.17	1.60	15.20	12.30	21.20	18.30	0.30	36x48
717A	SQFP 14X20-216	16.80	13.60	22.80	19.60	0.17	1.60	15.20	12.90	21.20	18.90	0.30	36x48
720A	SQFP 20X28-176	22.80	19.60	30.80	27.60	0.30	1.60	21.20	17.50	29.20	25.50	0.50	48x66
721A	SQFP 20X28-184	22.80	19.60	30.80	27.60	0.30	1.60	21.20	18.50	29.20	26.50	0.50	48x66
722A	SQFP 20X28-224	22.80	19.60	30.80	27.60	0.25	1.60	21.20	18.00	29.20	26.00	0.40	48x66
723A	SQFP 20X28-232	22.80	19.60	30.80	27.60	0.25	1.60	21.20	18.80	29.20	26.80	0.40	48x66
724A	SQFP 20X28-300	22.80	19.60	30.80	27.60	0.17	1.60	21.20	18.30	29.20	26.10	0.30	48x66
725A	SQFP 20X28-308	22.80	19.60	30.80	27.60	0.17	1.60	21.20	18.90	29.20	26.70	0.30	48x66
730A	SQFP 28X40-256	30.80	27.60	42.80	39.60	0.30	1.60	29.20	25.50	41.20	37.50	0.50	66x88
731A	SQFP 28X40-264	30.80	27.60	42.80	39.60	0.30	1.60	29.20	26.50	41.20	38.50	0.50	66x88
732A	SQFP 28X40-324	30.80	27.60	42.80	39.60	0.25	1.60	29.20	26.00	41.20	38.00	0.40	66x88
733A	SQFP 28X40-332	30.80	27.60	42.80	39.60	0.25	1.60	29.20	26.80	41.20	38.80	0.40	66x88
734A	SQFP 28X40-432	30.80	27.60	42.80	39.60	0.17	1.60	29.20	26.10	41.20	38.10	0.30	66x88
735A	SQFP 28X40-440	30.80	27.60	42.80	39.60	0.17	1.60	29.20	26.70	41.20	38.70	0.30	66x88

Figure 3b SQFP/QFP (Rectangular) land pattern dimensions

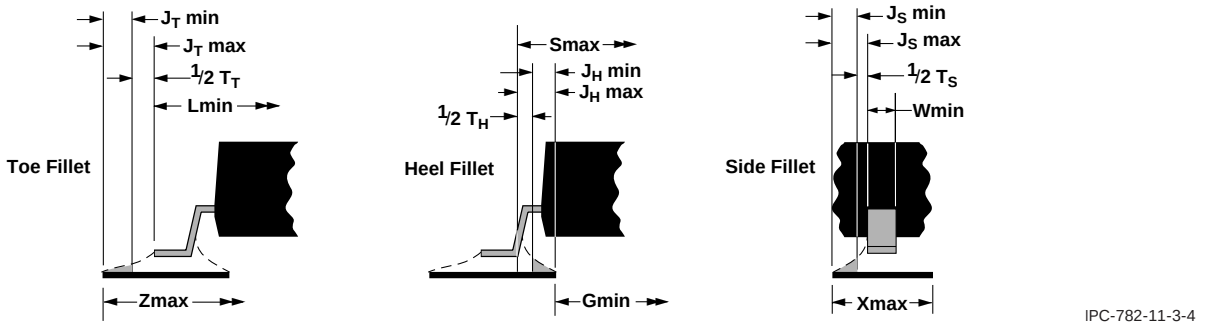
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint (Sides 1 and 2)								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
680/681A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
682/683A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
684/685A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
690/691A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
692/693A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
694/695A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
700/701A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
702/703A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
704/705A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
710A	0.10	0.10	0.57	0.27	0.53	0.76	0.22	0.58	0.32	-0.00	0.10
711A	0.10	0.10	0.57	0.27	0.53	0.76	0.22	0.58	0.33	-0.02	0.09
712/713A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
714/715A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
716/717A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
720/721A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
722/723A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
724/725A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
730/731A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
732/733A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
734/735A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for ceramic quad flat pack (CQFP) components. Basic construction of the CQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

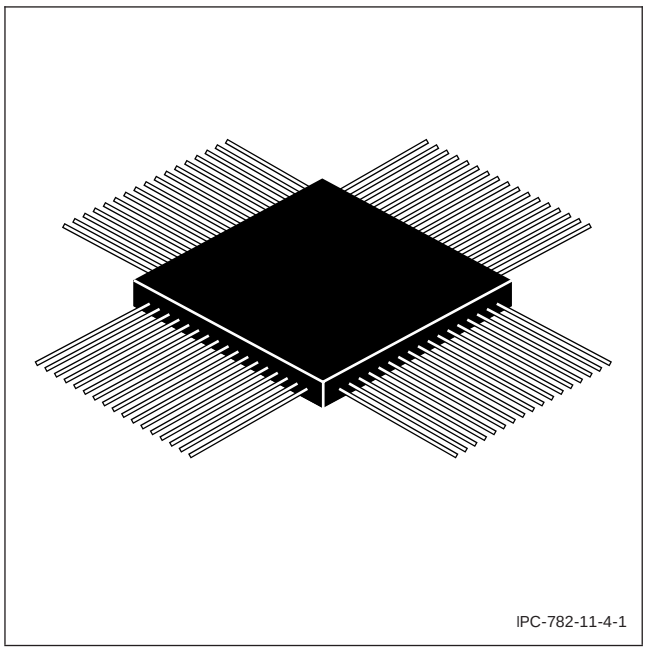
2.0 APPLICABLE DOCUMENTS

JEDEC Publication 95 Registered and Standard Outlines for Solid JEDEC Publication 95 State and Related Products, Outline MS 044

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Leaded ceramic chip carriers are typically supplied with an open cavity for chip placement. Ceramic or metal lids are soldered, epoxied, or attached with glass frit around the cavity to provide a hermetic seal.

An exception to this construction is the JEDEC standard MS044, which has the chip bonded to a lead frame, which is then sealed between two ceramic bodies with glass frit, similar to CERDIP fabrication. The ceramic packages are available in 28- through 196-lead configurations, with 1.27, 0.80, and 0.64 mm center spacing.



CQFP construction

Pre-leaded ceramic chip carriers typically have copper alloy or Kovar leads that are attached by the manufacturer. Leads are typically bonded to metallization on the top surface of the chip carrier. However, leads can be attached to the package castellations as well. Brazing or thermocompression bonding is usually the attachment means.

Pre-leaded packages using lead-frame construction are also available. These chip carriers have ceramic bodies with two opposing halves which mate above and below a lead frame to which the chip has been previously bonded. The seal is preformed with glass frit.

Leads can be formed to different shapes, such as ''J,'' ''L,'' or ''C'' configurations. Leads bent in the ''L'' configuration are known as ''gullwings.''

Pre-leaded chip carriers may be supplied with leads straight and attached to a common strip. The user must detach the common strip and form the leads to the desired configuration. This is done to minimize lead bending during shipping and handling. Leads may be supplied pre-tinned or with gold plating, as is often done for packages intended for a high reliability user.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

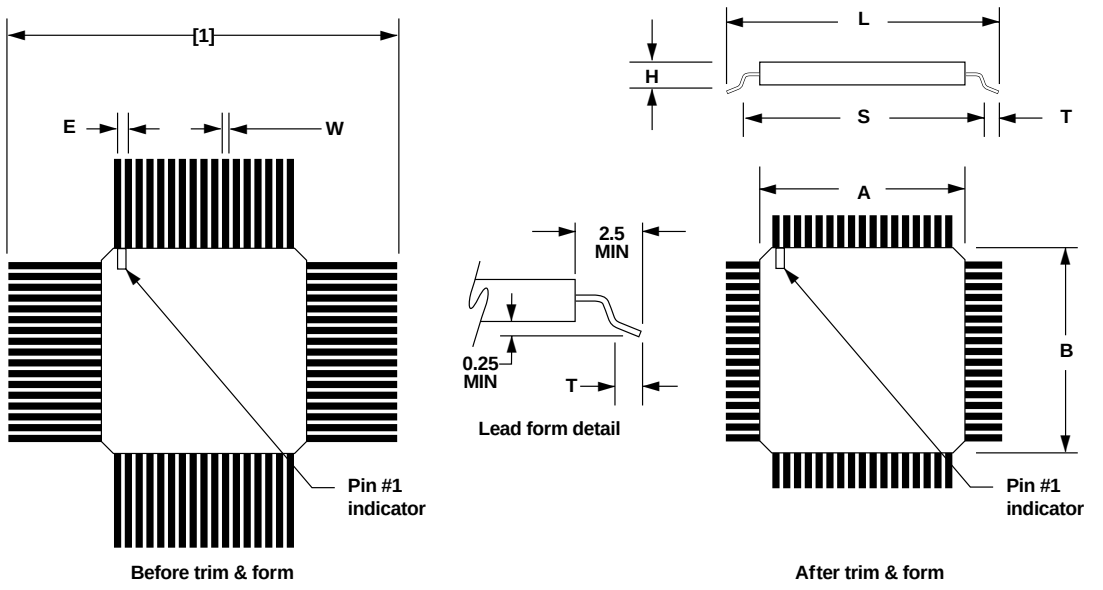
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. Pin 1 location may be molded into the plastic body.

3.1.3 Carrier Package Format Tube carriers are preferred for best handling.

3.1.4 Process Considerations CQFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for CQFP components.



The industry standard for the ceramic quad flat pack device family is not well defined.
The above details represent several configurations considered common but other sizes are available

IPC-782-11-4-2

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	max	basic
CQFP-28	14.40	14.80	11.86	12.39	0.32	0.48	1.02	1.27	9.05	10.05	9.05	10.05	2.30	1.270
CQFP-36	17.15	17.39	14.61	15.04	0.20	0.33	1.02	1.27	11.69	12.70	11.69	12.70	4.92	1.270
CQFP-44	19.69	19.93	17.15	17.58	0.20	0.33	1.02	1.27	14.23	15.24	14.23	15.24	4.92	1.270
CQFP-52	22.23	22.47	19.69	20.12	0.20	0.33	1.02	1.27	16.77	17.78	16.77	17.78	4.92	1.270
CQFP-68	27.31	27.55	24.77	25.20	0.20	0.33	1.02	1.27	21.85	22.86	21.85	22.86	4.92	1.270
CQFP-84	32.39	32.63	29.85	30.28	0.20	0.33	1.02	1.27	26.93	27.94	26.93	27.94	4.92	1.270
CQFP-100	37.47	37.71	34.93	35.36	0.20	0.33	1.02	1.27	32.01	33.02	32.01	33.02	4.92	1.270
CQFP-120	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-128	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-132	27.28	27.58	25.08	25.72	0.15	0.38	0.70	1.10	23.75	24.38	23.75	24.38	3.55	0.635
CQFP-144	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-148	33.50	34.00	30.96	31.57	0.12	0.25	1.02	1.27	28.21	28.71	28.21	28.71	3.10	0.635
CQFP-160	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-164	33.50	34.00	30.96	31.57	0.12	0.25	1.02	1.27	28.80	29.30	28.80	29.30	3.35	0.635
CQFP-196	35.75	36.25	33.21	33.82	0.12	0.25	1.02	1.27	33.80	34.30	33.80	34.30	3.45	0.635

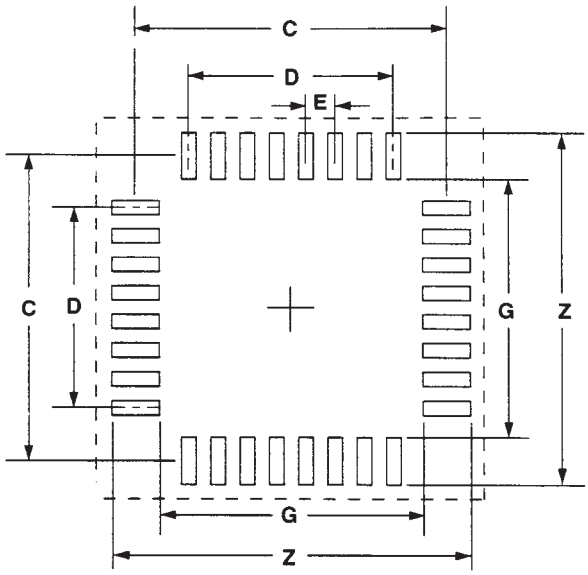
Figure 2 CQFP component dimensions

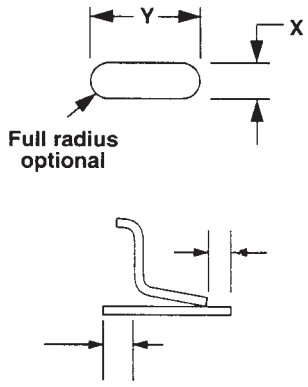
5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for CQFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.





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RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
750A	CQFP-28	15.80	10.60	0.65	2.60	13.20	7.62	1.27	34x34
751A	CQFP-36	18.60	13.80	0.65	2.40	16.20	10.16	1.27	40x40
752A	CQFP-44	21.00	16.20	0.65	2.40	18.60	12.70	1.27	44x44
753A	CQFP-52	23.60	18.80	0.65	2.40	21.20	15.24	1.27	50x50
754A	CQFP-68	28.60	23.80	0.65	2.40	26.20	20.32	1.27	62x62
755A	CQFP-84	33.80	29.00	0.65	2.40	31.40	25.40	1.27	70x70
756A	CQFP-100	38.80	34.00	0.65	2.40	36.40	30.48	1.27	80x80
757A	CQFP-120	32.40	28.00	0.50	2.20	30.20	23.20	0.80	68x68
758A	CQFP-128	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
759A	CQFP-132	28.60	24.20	0.40	2.20	26.40	20.32	0.64	60x60
760A	CQFP-144	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
761A	CQFP-148	35.20	30.00	0.35	2.60	32.60	22.86	0.64	72x72
762A	CQFP-160	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
763A	CQFP-164	35.20	30.00	0.35	2.60	32.60	25.40	0.64	72x72
764A	CQFP-196	37.20	32.00	0.35	2.60	34.60	30.48	0.64	76x76

Figure 3 CQFP land pattern dimensions

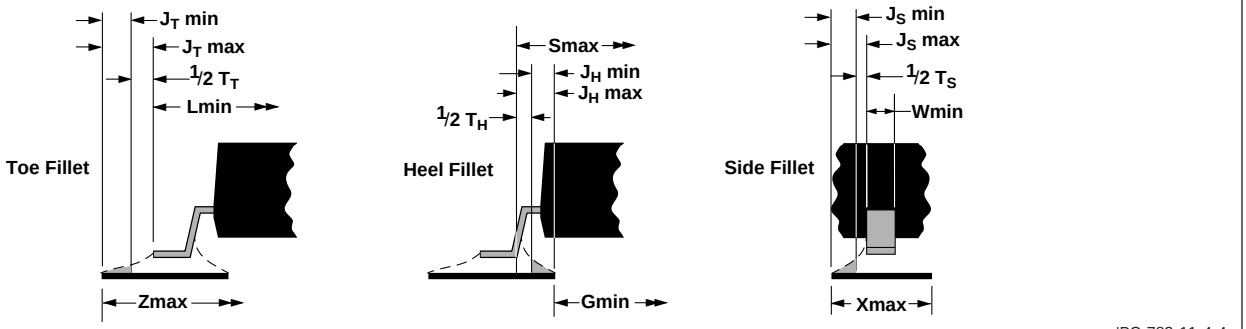
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
750A	0.10	0.10	0.40	0.46	0.70	0.53	0.59	0.90	0.16	0.00	0.17
751A	0.10	0.10	0.24	0.54	0.72	0.43	0.36	0.62	0.13	0.07	0.23
752A	0.10	0.10	0.24	0.47	0.65	0.43	0.43	0.69	0.13	0.07	0.23
753A	0.10	0.10	0.24	0.50	0.68	0.43	0.40	0.66	0.13	0.07	0.23
754A	0.10	0.10	0.24	0.46	0.64	0.43	0.44	0.70	0.13	0.07	0.23
755A	0.10	0.10	0.24	0.52	0.70	0.43	0.38	0.64	0.13	0.07	0.23
756A	0.10	0.10	0.24	0.48	0.66	0.43	0.42	0.68	0.13	0.07	0.23
757A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
758A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
759A	0.10	0.10	0.30	0.49	0.66	0.64	0.43	0.76	0.23	–0.01	0.13
760A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
761A	0.10	0.10	0.50	0.59	0.85	0.61	0.47	0.79	0.13	0.02	0.12
762A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
763A	0.10	0.10	0.50	0.59	0.85	0.61	0.47	0.79	0.13	0.02	0.12
764A	0.10	0.10	0.50	0.47	0.73	0.61	0.60	0.91	0.13	0.02	0.12

Figure 4 Tolerance and solder joint analysis

1.0 INTRODUCTION

This section covers land patterns for components with J leads on four sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description Leaded Chip Carriers are either ceramic or plastic packages with terminations which extend beyond the package outlines. These terminations typically space the body of the package from the packaging and interconnect structure for reasons of cleaning, inspecting, or accommodating differences in thermal expansion. The leads may be attached to the package body either before or after chip attachment.

In plastic leaded chip carriers, the primary packaging distinction concerns the point in which a chip is incorporated into the package. A pre-molded package is supplied as a leaded body with an open cavity for chip attachment. A post-molded body part typically has the chip attached to a lead frame with an insulating plastic body molded around the assembly. It is supplied from the manufacturer without apertures.

Leaded ceramic chip carriers may be similarly classified, but with a difference in category. The distinction concerns the point at which leads, if desired, are attached to the ceramic body. A pre-leaded ceramic chip carrier is supplied with copper or Kovar leads brazed to metallization integral with the ceramic package. Typically, the package is supplied with an open cavity for chip attach. A metal or ceramic lid is epoxied, soldered, or attached with glass frit to provide a hermetic seal around the chip. After these steps, the leaded assembly is attached to the printed board.

A post-leaded ceramic chip carrier typically has leads soldered to metallization on the ceramic package after chip attachment. These leads may take the form of edge clips or solder columns. Incorporation of leads into the assembly typically occurs immediately prior to board attachment.

High lead-end coplanarity in surface-mounted lead chip carriers is an important factor in reliable solder attachment to the printed board. Planarity may be measured from the lowest three leads of a leaded package. Coplanarity of 0.1 mm [0.004 in] maximum is recommended with 0.05 mm [0.002 in] preferred.

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1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copes should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	**12.1**
Revision	Subject
A	**PLCC (Square)**

1.0 SCOPE

This subsection provides the component and land pattern dimensions for plastic leaded chip carriers, square (PLCC components) with J leads on four sides. Basic construction of the PLCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Plastic Chip Carrier (PLCC) Family, 1.27 mm [0.050 in] Lead Spacing, Square,'' Outline MO-047, issue ''B,'' dated 11/88

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C or 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages.

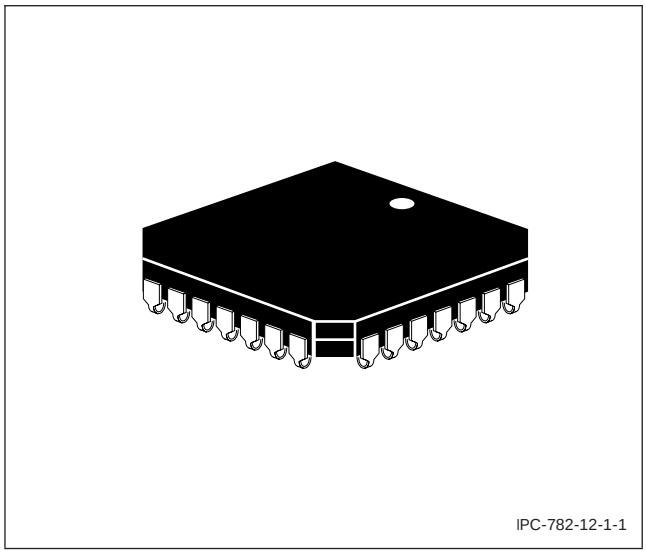


Figure 1 PLCC (Square)

3.1.1 Pre-molded Plastic Chip Carriers The pre-molded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

3.1.2 Post-molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the pre-molded package which has an aperture for mounting micro-electronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages which have J-lead configuration and are JEDC standard MO-047, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

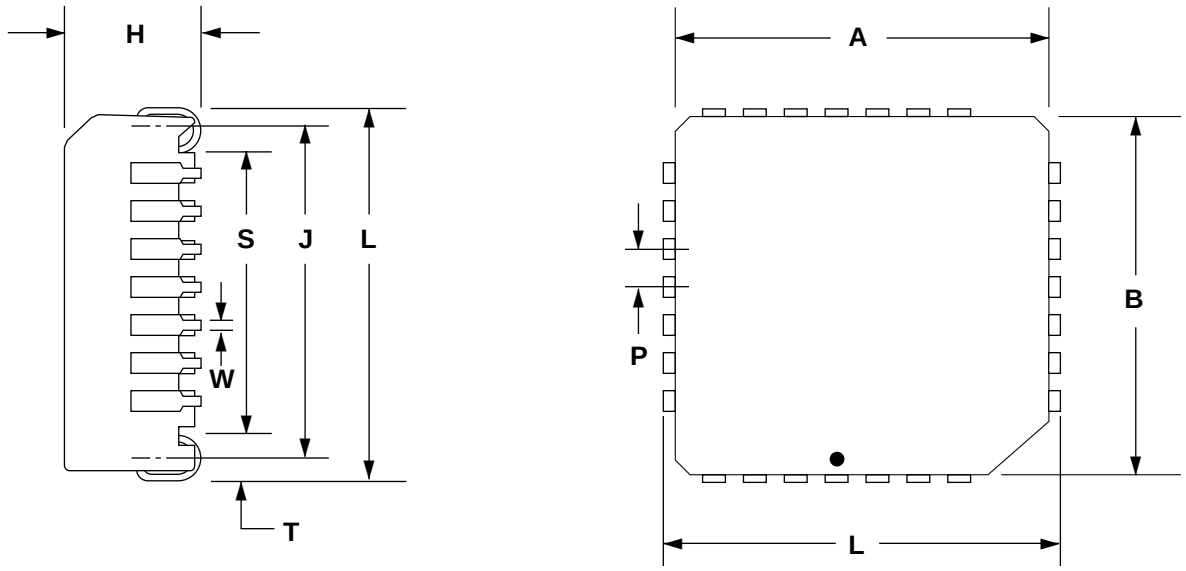
3.1.3 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.4 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.5 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PLCC (Square) components.



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Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		J (mm)	H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	ref	max	basic
PLCC-20	9.78	10.03	5.78	6.53	0.33	0.53	1.50	2.00	8.89	9.04	8.89	9.04	7.87	4.57	1.27
PLCC-28	12.32	12.57	8.32	9.07	0.33	0.53	1.50	2.00	11.43	11.58	11.43	11.58	10.41	4.57	1.27
PLCC-44	17.40	17.65	13.40	14.15	0.33	0.53	1.50	2.00	16.51	16.66	16.51	16.66	15.49	4.57	1.27
PLCC-52	19.94	20.19	15.94	16.69	0.33	0.53	1.50	2.00	19.05	19.20	19.05	19.20	18.03	5.08	1.27
PLCC-68	25.02	25.27	21.02	21.77	0.33	0.53	1.50	2.00	24.13	24.33	24.13	24.33	23.11	5.08	1.27
PLCC-84	30.10	30.35	26.10	26.85	0.33	0.53	1.50	2.00	29.21	29.41	29.21	29.41	28.19	5.08	1.27
PLCC-100	35.18	35.43	31.18	31.93	0.33	0.53	1.50	2.00	34.29	34.49	34.29	34.49	33.27	5.08	1.27
PLCC-124	42.80	43.05	38.80	39.55	0.33	0.53	1.50	2.00	41.91	42.11	41.91	42.11	40.89	5.08	1.27

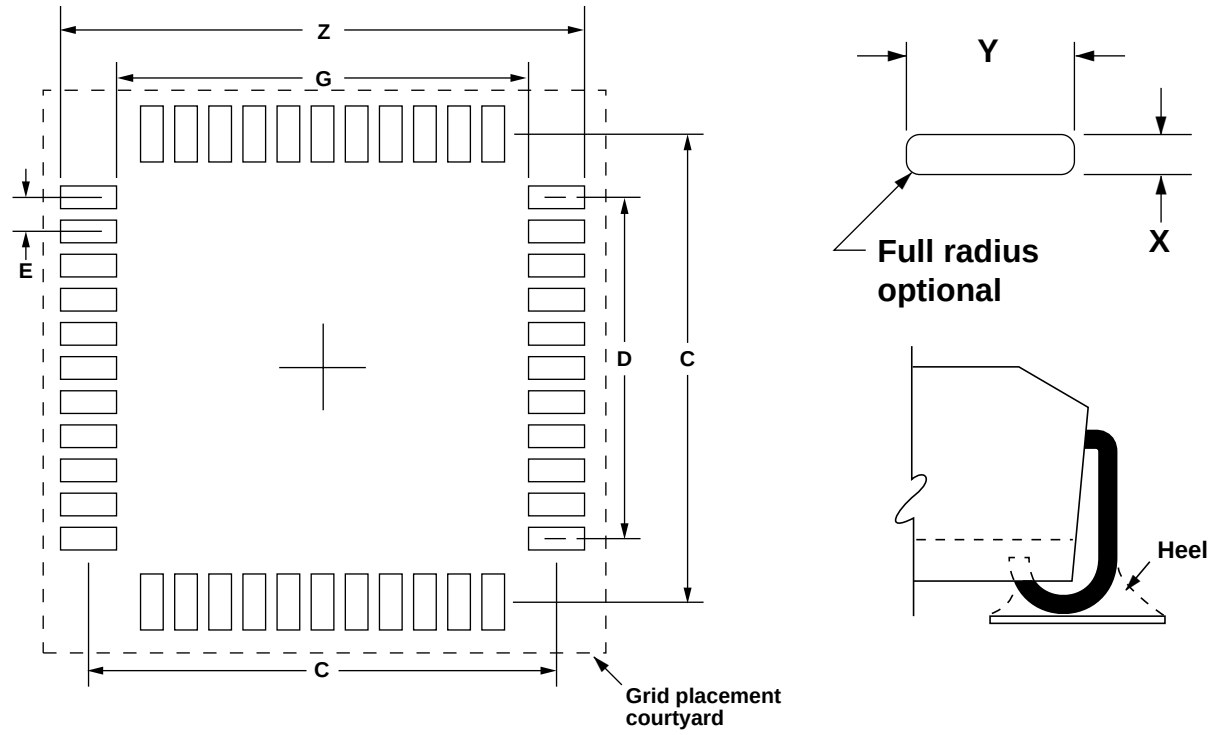
Figure 2 PLCC (Square)

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PLCC (Square) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
790A	PLCC-20	10.80	6.40	0.60	2.20	8.60	5.08	1.27	24x24
791A	PLCC-28	13.40	9.00	0.60	2.20	11.20	7.62	1.27	30x30
792A	PLCC-44	18.40	14.00	0.60	2.20	16.20	12.70	1.27	40x40
793A	PLCC-52	21.00	16.60	0.60	2.20	18.80	15.24	1.27	44x44
794A	PLCC-68	26.00	21.60	0.60	2.20	23.80	20.32	1.27	54x54
795A	PLCC-84	31.20	26.80	0.60	2.20	29.00	25.40	1.27	66x66
796A	PLCC-100	36.20	31.80	0.60	2.20	34.00	30.48	1.27	76x76
797A	PLCC-124	43.80	39.40	0.60	2.20	41.60	38.10	1.27	90x90

Figure 3 PLCC (Square) land pattern dimensions

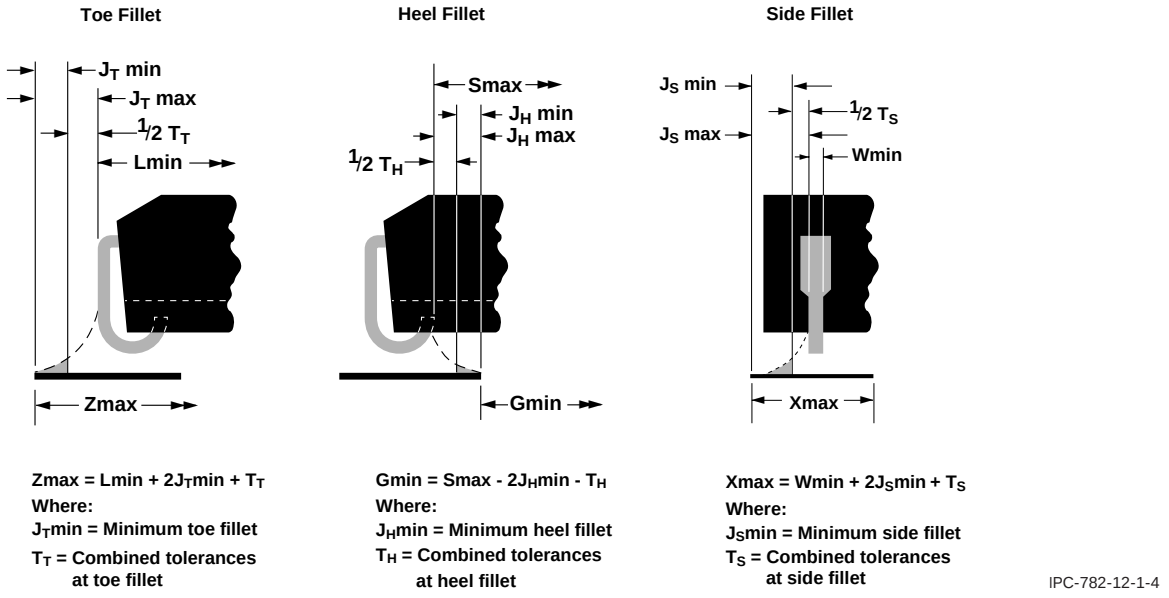
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be asgiven in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint								
			Heel (mm)			Toe (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_H$min	$J_H$max	C_S	$J_T$min	$J_T$max	C_W	$J_S$min	$J_S$max
790A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
791A	0.10	0.10	0.25	0.40	0.54	0.75	-0.35	0.04	0.20	0.01	0.14
792A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14
793A	0.10	0.10	0.25	0.39	0.53	0.75	-0.34	0.04	0.20	0.01	0.14
794A	0.10	0.10	0.25	0.35	0.49	0.75	-0.30	0.08	0.20	0.01	0.14
795A	0.10	0.10	0.25	0.41	0.55	0.75	-0.36	0.03	0.20	0.01	0.14
796A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
797A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for plastic leaded chip carriers, rectangular (PLCC components) with J leads on four sides. Basic construction of the PLCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Plastic Chip Carrier (PLCC) Family, 1.27 mm [0.050 in] Lead Spacing, Square,'' Outline MO-052, issue ''B,'' dated 8/85

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C or 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages.

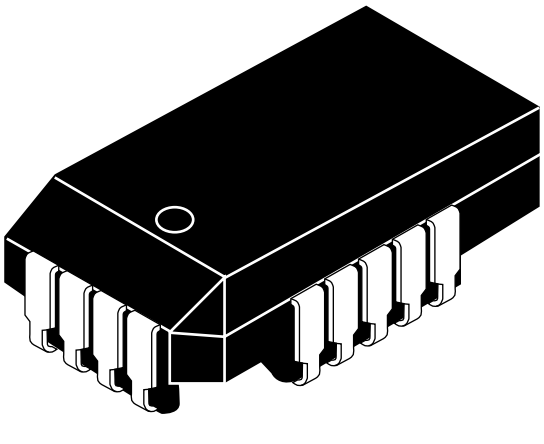


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Figure 1 PLCC (Rectangular) construction

3.1.1 Pre-molded Plastic Chip Carriers The pre-molded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to mae use of silicone encapsulant technology for chip coverage and protection.

3.1.2 Post-molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the pre-molded package which has an aperture for mounting micro-electronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages which have J-lead configuration and are JEDC standard MO-052, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

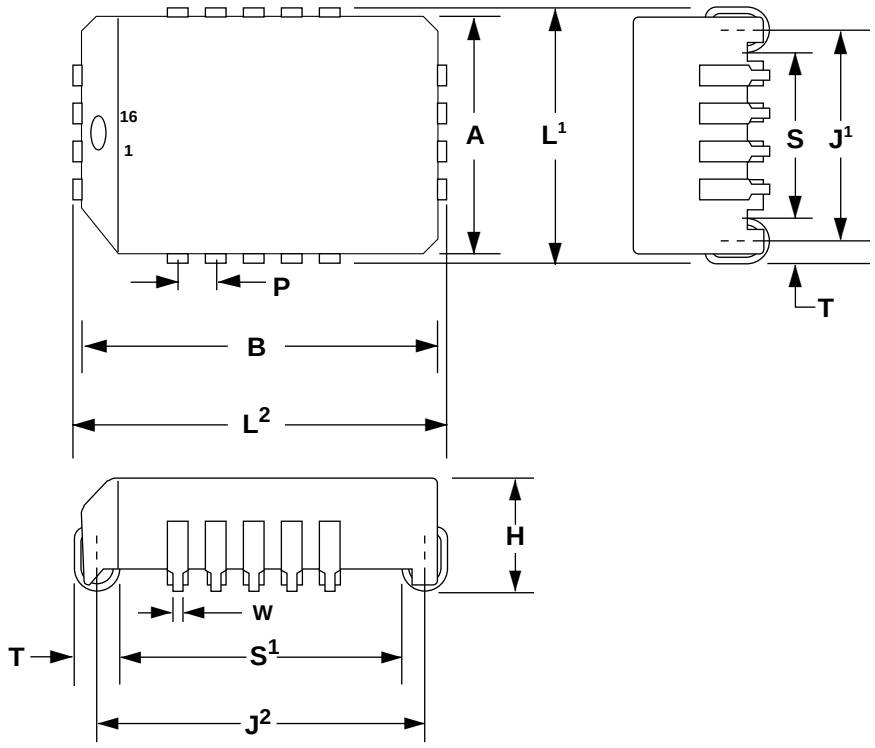
3.1.3 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.4 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.5 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PLCC (Rectangular) components.



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Component Identifier	L1 (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		A (mm)	B (mm)	J1 (mm)	J2 (mm)	H (mm)	P (mm)	Pin Count, Short Side	Pin Count, Long Side
	min	max	min	max	min	max	min	max	m in	max	min	max	max	max	ref	ref	max	basic		
PLCC/R-18	8.05	8.30	4.05	4.80	11.61	11.86	7.61	8.36	0.33	0.53	1.50	2.00	7.32	10.87	6.20	9.75	3.57	1.27	4	5
PLCC/R- 18L	8.13	8.51	4.13	4.93	13.21	13.59	9.21	10.01	0.33	0.53	1.50	2.00	7.44	12.52	6.20	11.25	3.57	1.27	4	5
PLCC/R- 22	8.13	8.51	4.13	4.93	13.21	13.59	9.21	10.01	0.33	0.53	1.50	2.00	7.44	12.52	6.20	11.25	3.57	1.27	4	7
PLCC/R-28	9.78	10.03	5.78	6.53	14.86	15.11	10.86	11.61	0.33	0.53	1.50	2.00	8.97	14.05	7.90	12.95	3.57	1.27	5	9
PLCC/R- 32	12.32	12.57	8.32	9.07	14.86	15.11	10.86	11.61	0.33	0.53	1.50	2.00	11.51	14.05	10.40	12.95	3.57	1.27	7	9

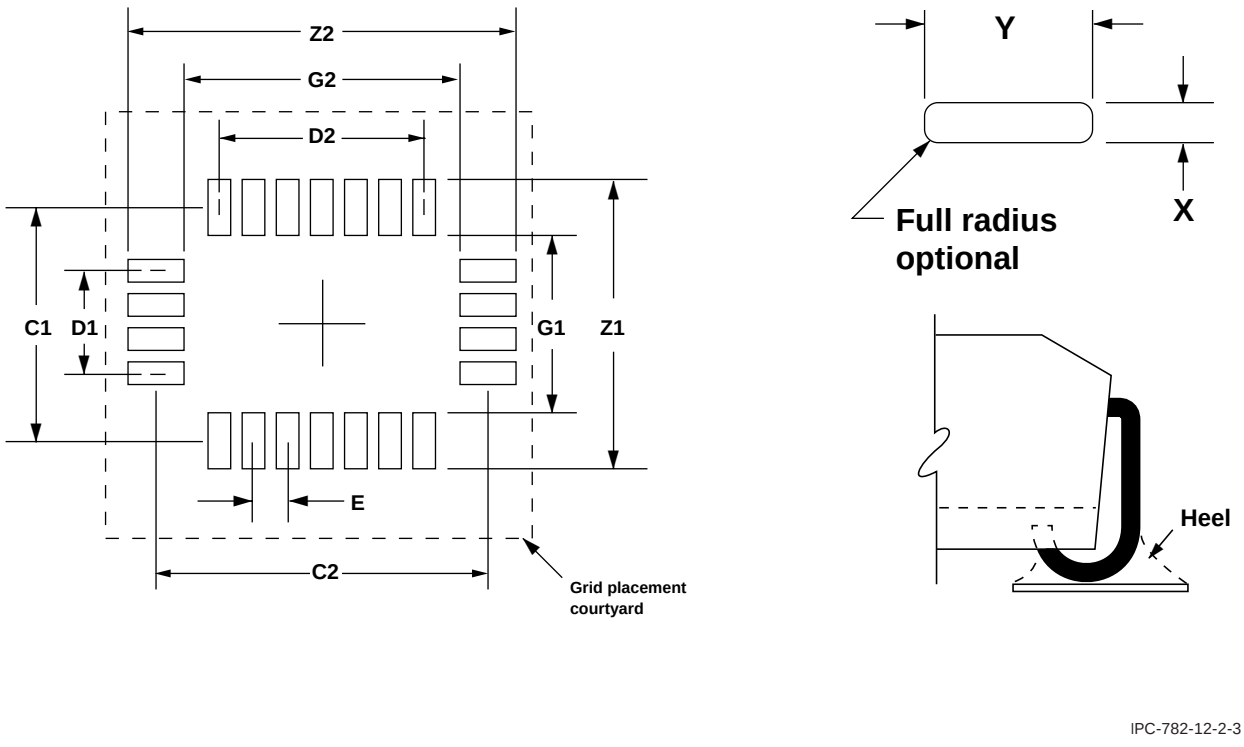
Figure 2 PLCC (Rectangular) component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PLCC (Rectangular) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm) ref	C1 (mm) ref	C2 (mm) ref	D1 (mm) ref	D2 (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements
810A	PLCC/R-18	9.40	5.00	12.80	8.40	0.60	2.00	7.20	10.60	3.81	5.08	1.27	22x28
811A	PLCC/R-18-L	9.40	5.00	14.40	10.00	0.60	2.00	7.20	12.20	3.81	5.08	1.27	22x32
812A	PLCC/R-22	9.40	5.00	14.40	10.00	0.60	2.00	7.20	12.20	3.81	7.62	1.27	22x32
813A	PLCC/R-28	11.00	6.60	16.00	11.60	0.60	2.00	8.80	13.80	5.08	10.16	1.27	24x34
814A	PLCC/R-32	13.60	9.20	16.00	11.60	0.60	2.00	11.40	13.80	7.62	10.16	1.27	30x34

Figure 3 PLCC (Rectangular) land pattern dimensions

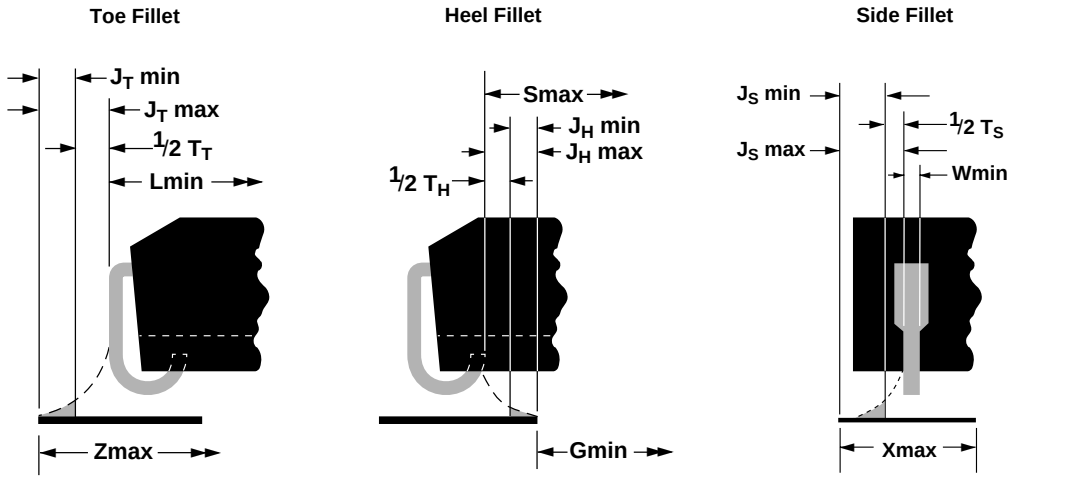
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be asgiven in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Zmax = Lmin + 2$J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet

Gmin = Smax - 2$J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet

Xmax = Wmin + 2$J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

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RLP No.	Tolerance Assumptions (mm)		Solder Joint												
			Heel 1 and 2 (mm)					Toe 1 and 2 (mm)					Side 1 and 2 (mm)		
	F	P	C_L	J_{H1}min	J_{H1}max	J_{H2}min	J_{H2}max	C_S	J_{T1}min	J_{T1}max	J_{T2}min	J_{T2}max	C_W	$J_S$min	$J_S$max
810A	0.10	0.10	0.25	0.53	0.67	0.45	0.60	0.75	–0.48	–0.10	–0.40	–0.02	0.20	0.01	0.14
811A	0.10	0.10	0.38	0.43	0.64	0.39	0.60	0.80	–0.44	–0.03	–0.40	0.01	0.20	0.01	0.14
812A	0.10	0.10	0.38	0.43	0.64	0.39	0.60	0.80	–0.44	–0.03	–0.40	0.01	0.20	0.01	0.14
813A	0.10	0.10	0.25	0.47	0.61	0.43	0.57	0.75	–0.42	–0.04	–0.38	0.00	0.20	0.01	0.14
814A	0.10	0.10	0.25	0.50	0.64	0.43	0.57	0.75	–0.45	–0.06	–0.38	0.00	0.20	0.01	0.14

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for leadless ceramic chip carriers (LCC components). Basic construction of the LCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95

Registered and Standard Outlines for Solid JEDEC Publication 95 State and Related Products, ''0.050 In. Center, Leadless Type A,'' Outline MS002, issue ''A,'' dated 9/29/80, and ''0.050 In. Center, Leadless Type C,'' Outline MS004, issue ''B,'' dated 5/90

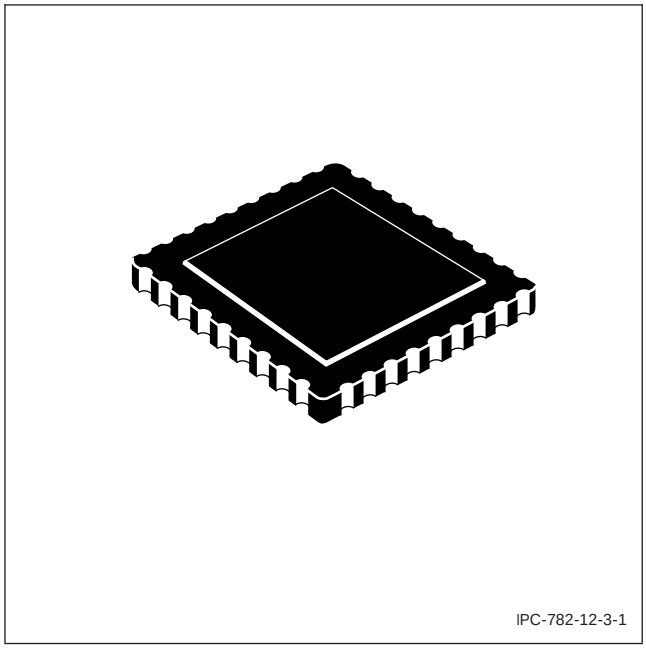


Figure 1 LCC Construction

3.0 Component Descriptions

3.1 Basic Construction A leadless chip carrier is a ceramic package with integral surface-metallized terminations. Leadless Types A, B, and D chip carriers have a chamfered index corner that is larger than that of Type C. Another difference between the A, B, and D types and Type C is the feature in the other three corners. The types A, B, and D, were designed for socket applications and printed wiring interconnections. The Type C is primarily intended for direct attachment through reflow soldering. This application difference is the main reason for their mechanical differences. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation.

Leadless Type A is intended for lid-down mounting in a socket, which places the primary heat-dissipating surface away from the mounting surface for more effective cooling in air-cooled systems.

Type C is a ceramic package similar to leadless Type B except for corner configuration. The 50 mil center family, which includes both leadless and leaded devices, is designed to mount on a common mounting pattern. They may be directly attached to the mounting structure, or can be plugged into sockets. One basic restriction is that there shall be no terminals in the corners of the package. There are a number of common sizes.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in.] thick.

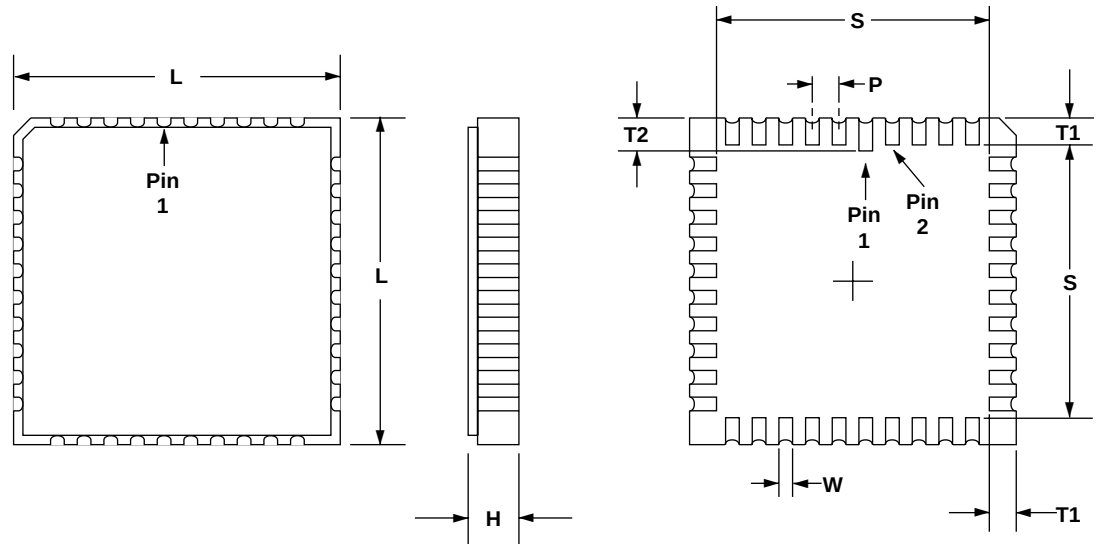
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. Pin 1 location may be molded into the plastic body.

3.1.3 Carrier Package Format Tube carriers are preferred for best handling.

3.1.4 Process Considerations LCCs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for LCC components.



Note: Component body Widths normally described as "A" & "B" on other components are equal to "L".

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Component Identifier	Type	L (mm)		S (mm)		W (mm)		T1 (mm)		T2 (mm)		H (mm)	P (mm)
		min	max	min	max	min	max	min	max	m in	max	max	basic
LCC-16	Type C	7.42	7.82	4.64	5.16	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-20	Type C	8.69	9.09	5.91	6.43	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-24	Type C	10.04	10.41	7.26	7.76	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-28	Type C	11.23	11.63	8.45	8.97	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-44	Type C	16.26	16.76	13.48	14.08	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-52	Type C	18.78	19.32	16.00	16.64	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-68	Type C	23.83	24.43	21.05	21.74	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-84	Type C	28.83	29.59	26.05	26.88	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-100	Type A	34.02	34.56	31.24	31.88	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27
LCC-124	Type A	41.64	42.18	38.86	39.50	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27
LCC-156	Type A	51.80	52.34	49.02	49.66	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27

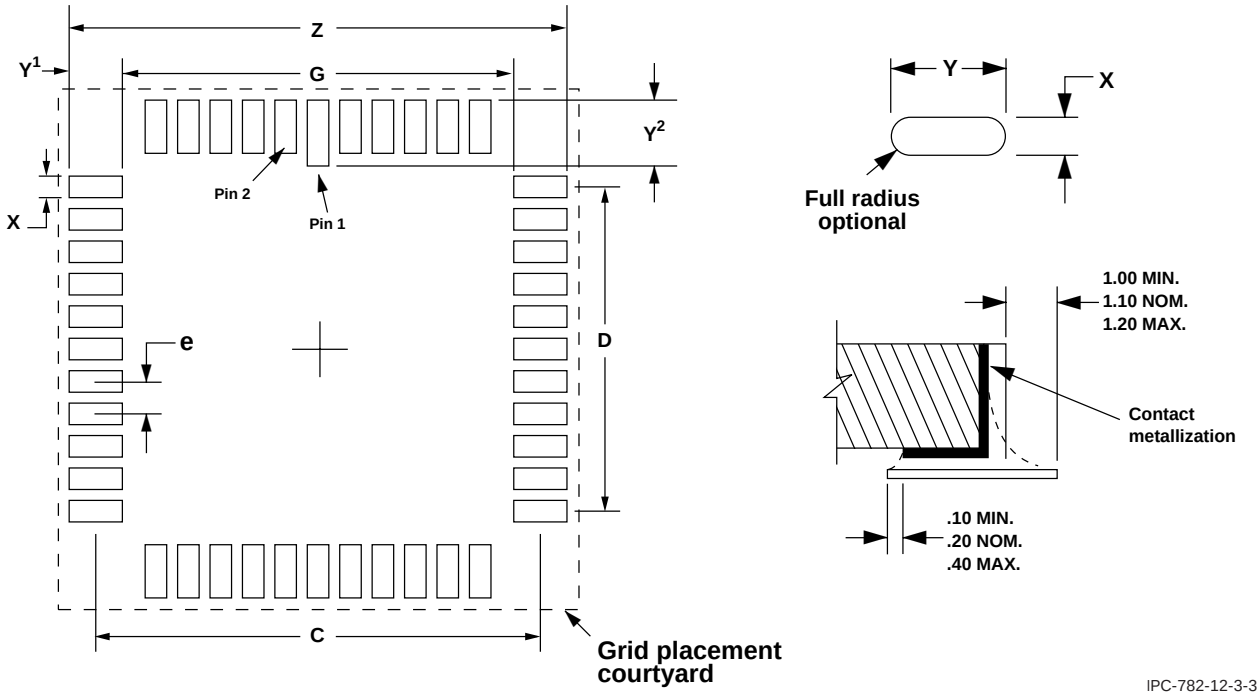
Figure 2 LCC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for LCC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y1 (mm) ref	Y2 (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
830	LCC-16	9.80	4.60	0.80	2.60	3.40	7.20	3.81	1.27	22X22
831	LCC-20	11.00	5.80	0.80	2.60	3.40	8.40	5.08	1.27	24X24
832	LCC-24	12.40	7.20	0.80	2.60	3.40	9.80	6.35	1.27	26X26
833	LCC-28	13.60	8.40	0.80	2.60	3.40	11.00	7.62	1.27	30X30
834	LCC-44	18.80	13.60	0.80	2.60	3.40	16.20	12.70	1.27	40X40
835	LCC-52	21.20	16.00	0.80	2.60	3.40	18.60	15.24	1.27	44X44
836	LCC-68	26.20	21.00	0.80	2.60	3.40	23.60	20.32	1.27	54X54
837	LCC-84	31.40	26.20	0.80	2.60	3.40	28.80	25.40	1.27	64X64
838	LCC-100	36.40	31.20	0.80	2.60	3.40	33.80	30.48	1.27	74X74
839	LCC-124	44.20	39.00	0.80	2.60	3.40	41.60	38.10	1.27	90X90
840	LCC-156	54.20	49.00	0.80	2.60	3.40	51.60	48.26	1.27	110X110

Figure 3 LCC land pattern dimensions

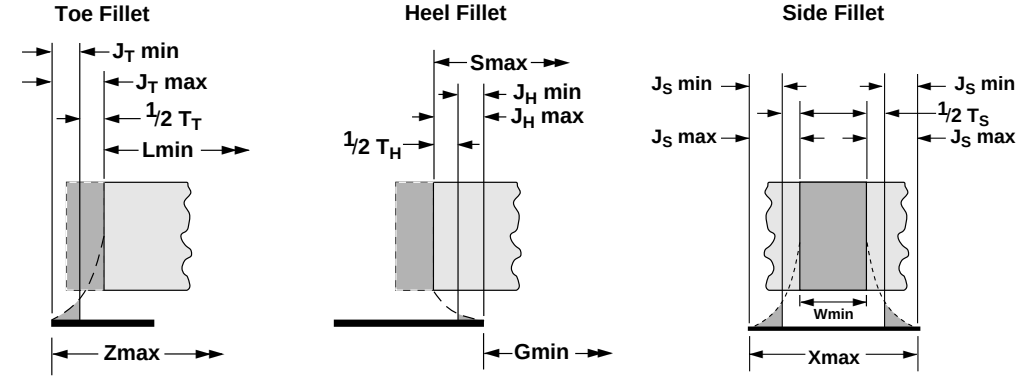
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



$Z_{max} = L_{min} + 2J_T min + T_T$
Where:
$J_T min$ = Minimum toe fillet
T_T = Combined tolerances at toe fillet

$G_{min} = S_{max} - 2J_H min - T_H$
Where:
$J_H min$ = Minimum heel fillet
T_H = Combined tolerances at heel fillet

$X_{max} = W_{min} + 2J_S min + T_S$
Where:
$J_S min$ = Minimum side fillet
T_S = Combined tolerances at side fillet

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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T min$	$J_T max$	C_S	$J_H min$	$J_H max$	C_W	$J_S m in$	$J_S max$
830	0.20	0.20	0.40	0.95	1.19	0.525	–0.02	0.28	0.480	–0.16	0.12
831	0.20	0.20	0.40	0.91	1.15	0.525	0.02	0.32	0.480	–0.16	0.12
832	0.20	0.20	0.37	0.95	1.18	0.502	–0.01	0.28	0.480	–0.16	0.12
833	0.20	0.20	0.40	0.94	1.18	0.525	–0.01	0.29	0.480	–0.16	0.12
834	0.20	0.20	0.50	0.98	1.27	0.604	–0.09	0.24	0.480	–0.16	0.12
835	0.20	0.20	0.54	0.91	1.21	0.638	-0.03	0.32	0.480	–0.16	0.12
836	0.20	0.20	0.60	0.85	1.19	0.689	–0.00	0.37	0.480	–0.16	0.12
837	0.20	0.20	0.76	0.88	1.28	0.832	–0.10	0.34	0.480	–0.16	0.12
838	0.20	0.20	0.54	0.89	1.19	0.638	–0.01	0.34	0.480	–0.16	0.12
839	0.20	0.20	0.54	0.98	1.28	0.638	–0.10	0.25	0.480	–0.16	0.12
840	0.20	0.20	0.54	0.90	1.20	0.638	–0.02	0.33	0.480	–0.16	0.12

Figure 4 Tolerance and solder joint analysis

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Surface Mount Design and Land Pattern Standard

Date	Section
8/93	**13.0**
Revision	Subject
	DIPs

1.0 INTRODUCTION

This section covers land patterns for DIPs (Modified Dual-In-Line components). Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents
Modified Dual-In-Line Components

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-2 16 mm and 24 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication Registered and Standard Outlines for Solid State and Related Products:

Outline	Issue	Title
MS-001	C	Standard Dual-In-Line Family, 0.300 in. Row Spacing (Plastic)
MS-010	B	Standard Dual-In-Line Family, 0.400 in. Row Spacing (Plastic)
MS-011	B	Standard Dual-In-Line Family, 0.600 in. Row Spacing (Plastic)

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 GENERAL INFORMATION

3.1 General Component Description A method of modifying DIPs for surface mounting is the ''I'' mounting technique. This involves simply cutting the DIP leads to a short length and placing the device on a pattern of lands to be soldered along with the other surface mounted devices.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copes should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for DIPs (Modified Dual-In-Line components). Basic construction of the DIP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 13.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Construction is usually made of plastic or ceramics.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

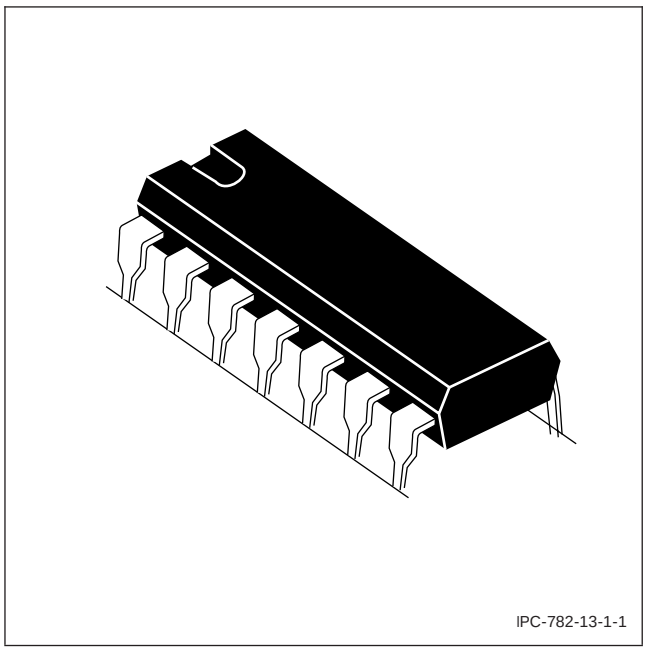


Figure 1 DIP construction

Solder finish applied over precious-metal leads shall have a diffusion-barrier layer between the lead metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

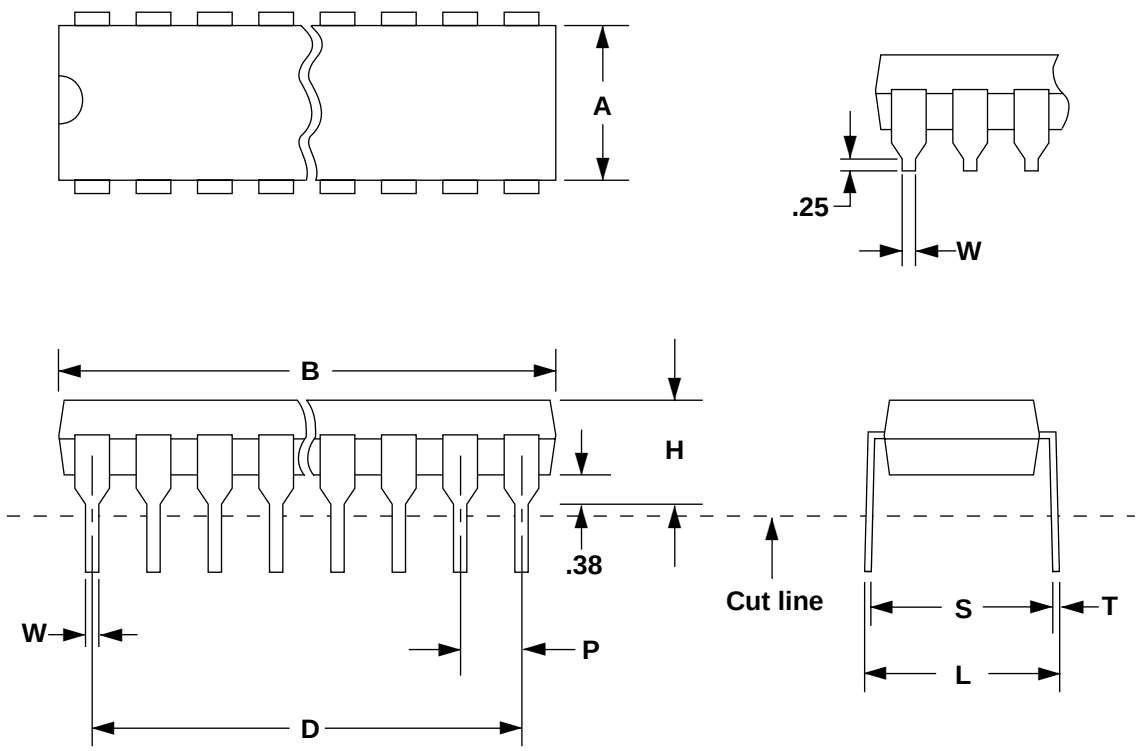
3.1.2 Marking Parts shall be marked with the part number and a date code. In addition, pin 1 shall be identified.

3.1.3 Carrier Package Format Carrier format may be tubes or as agreed to between user and vendor.

3.1.4 Resistance to Soldering The parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of a minimum of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for DIP components.



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	m in	max	min	max	max	basic
DIP 8	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	8.84	10.92	5.33	2.54
DIP 14	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	18.42	20.19	5.33	2.54
DIP 16	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	18.93	21.33	5.33	2.54
DIP 18	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	21.47	23.49	5.33	2.54
DIP 20	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	23.50	26.90	5.33	2.54
DIP 22L	9.91	10.79	9.15	10.07	0.36	0.56	0.20	0.38	8.39	9.65	26.67	28.44	5.33	2.54
DIP 24	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	28.60	32.30	5.33	2.54
DIP 24L	9.91	10.79	9.15	10.07	0.36	0.56	0.20	0.38	8.39	9.65	29.21	30.98	5.33	2.54
DIP 24X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	29.30	32.70	6.35	2.54
DIP 28	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	34.20	36.20	5.33	2.54
DIP 28X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	35.10	39.70	6.35	2.54
DIP 40X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	50.30	53.20	6.35	2.54
DIP 48X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	60.70	63.10	6.35	2.54

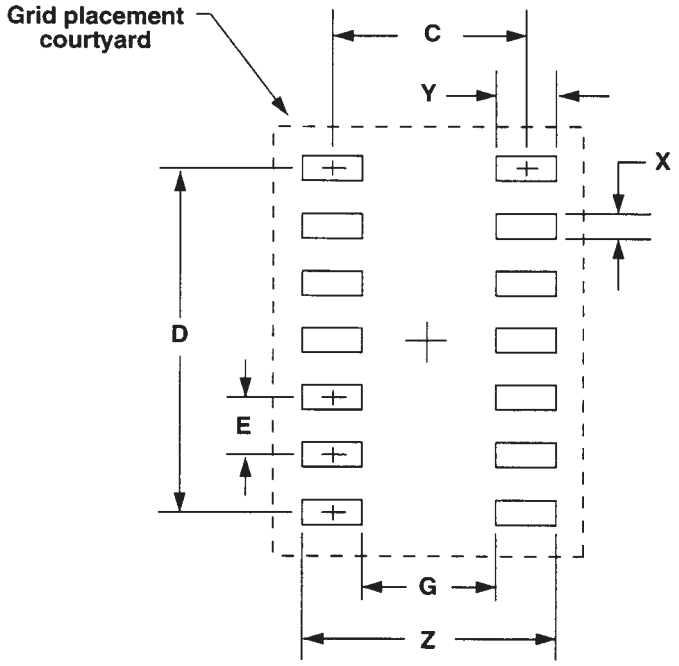
Figure 2 DIP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for DIP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



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RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
860	DIP 8	9.80	5.40	1.20	2.20	7.60	7.62	2.54	22x24
861	DIP 14	9.80	5.40	1.20	2.20	7.60	15.24	2.54	22x42
862	DIP 16	9.80	5.40	1.20	2.20	7.60	17.78	2.54	22x44
863	DIP 18	9.80	5.40	1.20	2.20	7.60	20.32	2.54	22x48
864	DIP 20	9.80	5.40	1.20	2.20	7.60	22.86	2.54	22x56
865	DIP 22L	12.40	8.00	1.20	2.20	10.20	25.40	2.54	26x58
866	DIP 24	9.80	5.40	1.20	2.20	7.60	27.94	2.54	38x66
867	DIP 24L	12.40	8.00	1.20	2.20	10.20	27.94	2.54	26x64
867	DIP 24X	17.40	13.00	1.20	2.20	15.20	27.94	2.54	36x68
869	DIP 28	9.80	5.40	1.20	2.20	7.60	33.02	2.54	22x74
870	DIP 28X	17.40	13.00	1.20	2.20	15.20	33.02	2.54	36x84
871	DIP 40X	17.40	13.00	1.20	2.20	15.20	48.26	2.54	36x110
872	DIP 48X	17.40	13.00	1.20	2.20	15.20	58.42	2.54	36x130

Figure 3 DIP land pattern dimensions

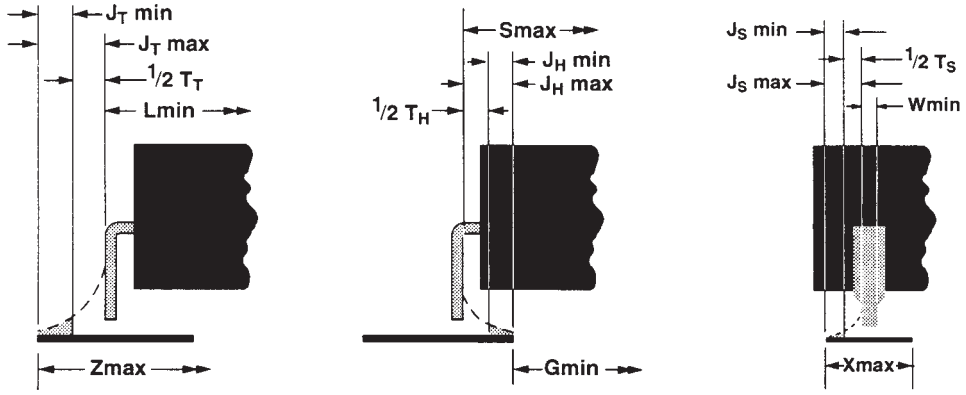
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



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	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
860	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
861	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
862	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
863	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
864	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
865	0.20	0.20	0.880	0.78	1.25	0.916	0.55	1.03	0.200	0.25	0.42
866	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
867	0.20	0.20	0.880	0.78	1.25	0.916	0.55	1.03	0.200	0.25	0.42
868	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
869	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
870	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
871	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
872	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42

Figure 4 Tolerance and solder joint analysis