Product Specification

(Preliminary)

Part Name: OEL Display Module
Customer Part ID:
WiseChip Part ID: UG-9696TDDCG02
Doc No.: SAS1-0J021-A

Customer:
Approved by

From: WiseChip Semiconductor Inc.
Approved by

WiseChip Semiconductor Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UG-9696TDDCG02	A	New	March 10, 2011

Contents

1. Basic Specifications

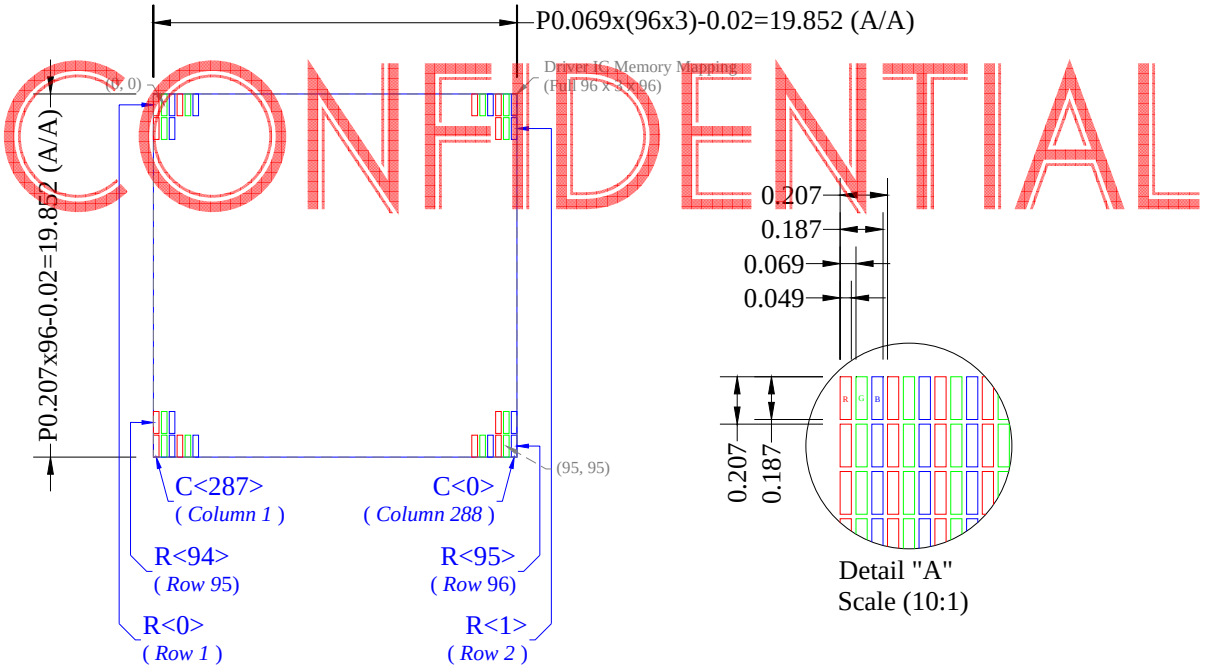
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: 65,536 Colors (Maximum)
3) Drive Duty: 1/96 Duty

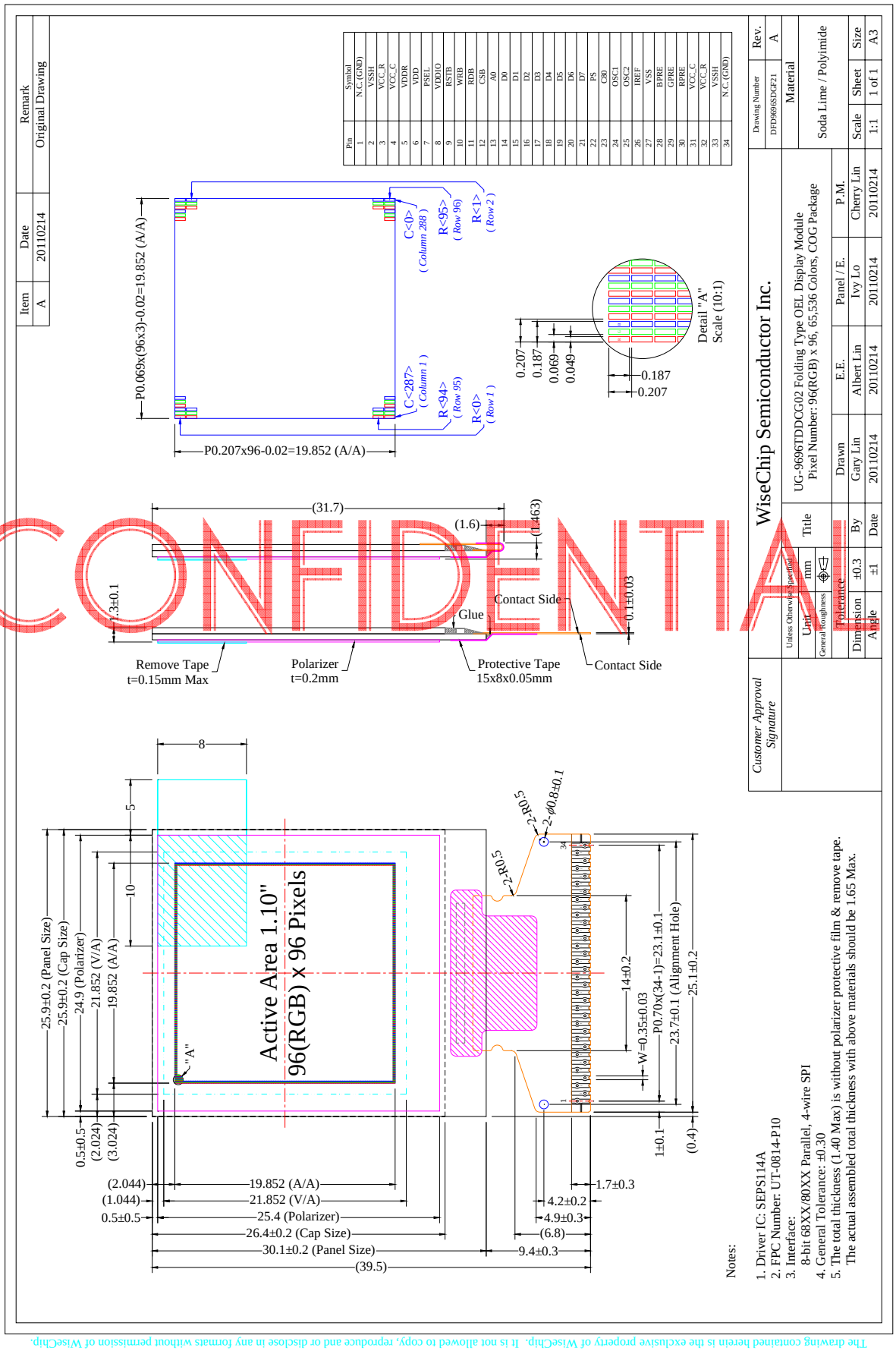
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 96 (RGB) × 96
3) Panel Size: 25.90 × 30.10 × 1.30 (mm)
4) Active Area: 19.852 × 19.852 (mm)
5) Pixel Pitch: 0.069 × 0.207 (mm)
6) Pixel Size: 0.049 × 0.187 (mm)
7) Weight: 2.07 (g)

1.3 Active Area / Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



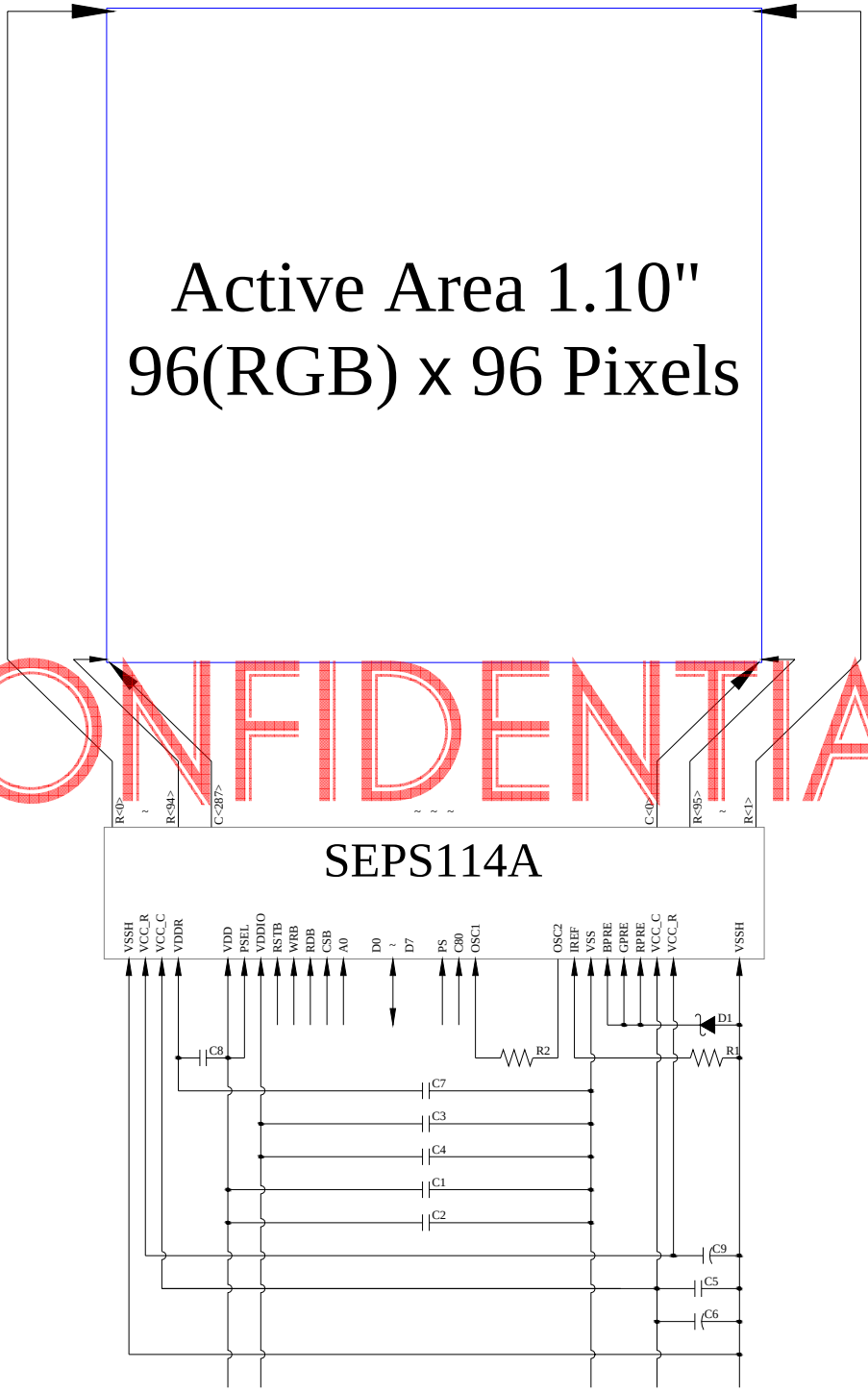
1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
6	VDD	P	**Power Supply for Operation** This is a voltage supply pin. It must be connected to external source.
5	VDDR	P	**Power Supply for Core Logic Circuit** This is a voltage supply pin. It can be supplied externally or regulated internally from V_{DD}. A capacitor should be connected between this pin & V_{SS} under all circumstances.
8	VDDIO	P	**Power Supply for I/O Pin** This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have V_{IH} reference to V_{DDIO}. When I/O signal pins (C80, PS, D0~D7, control signals…) pull high, they should be connected to V_{DDIO}.
27	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
4, 31	VCC_C	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
2, 33	VSSH	P	**Ground of OEL Panel** This is the ground pins for analog circuits. It must be connected to external ground.
Driver			
30 29 28	RPRE GPRE BPRE	I/O	**External Voltage Reference for Pre-charge Signal** This is the precharge driving voltages for OEL driving segment pins respectively. A zener diode should be connected between this pin and V_{SS}.
26	IREF	I/O	**Current Reference for Brightness Adjustment** This is the current reference pin to generate precharge and driving current. A 39kΩ resistor should be connected between this pin and V_{SS}.
3, 32	VCC_R	P	**Voltage Output High Level for Scan Signal** This is the scan driver power supply pin. A tantalum capacitor should be connected between this pin and V_{SS}.
Clock			
24 25	OSC1 OSC2	I O	**Fine Adjustment for Oscillation** The frequency is controlled by external 27kΩ resistor between OSC1 and OSC2. The oscillator signal is used for system clock generation. When the external clock mode is selected, OSC1 is used external clock input.
Configuration			
7	PSEL	I	**Regulator Enable/Disable for Logic Power Supply** This pin is the regulator enable/disable input of V_{DDR}. If it is connected to V_{DD}, the internal regulator is used. Otherwise, an external voltage supplier should be used.
Interface			
23	C80	I	**Select the CPU Type** Low: 80XX-Series MCU High: 68XX-Series MCU.
22	PS	I	**Select Parallel/Serial Interface Type** Low: Serial Interface High: Parallel Interface
9	RSTB	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed.
12	CSB	I	**Chip Select** Low: SEPS114A is selected and can be accessed. High: SEPS114A is not selected and cannot be accessed.
13	A0	I	**Data/Command Control** Low: Command High: Parameter/Data

1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface (Continued)</td></tr>
<tr><td>11</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
68XX Parallel Interface: Bus Enabled Strobe (Active High)
80XX Parallel Interface: Read Strobe Signal (Active Low)
While using SPI, it must be connected to V_{DD} or V_{SS}.</td></tr>
<tr><td>10</td><td>WRB</td><td>I</td><td>Write or Read/Write Select
68XX Parallel Interface: Read (Low)/Write (High) Select
80XX Parallel Interface: Write Strobe Signal (Active Low)
While using SPI, it must be connected to V_{DD} or V_{SS}.</td></tr>
<tr><td>14~21</td><td>D0~D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>0</td><td>D[0] SCL: Synchronous Clock Input
D[1] SDI: Serial Data Input
D[2] SDO: Serial Data Output
D[3] R/W: Serial Read (High)/Write (Low)</td></tr>
<tr><td>1</td><td>8-bit Bus: D[7:0]</td></tr>
</table>
While using SPI, the unused pins must be connected to V_{SS}.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 34</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
</table>

1.6 Block Diagram



MCU Interface Selection: PS, C80
Pins connected to MCU interface: RSTB, WRB, RDB, CSB, A0, and D0~D7

C1, C3, C5: 0.1μF
C2, C4, C8: 4.7μF
C6, C9: 4.7μF / 25V Tantalum Capacitor
C7: 2.2μF
R1: 39kΩ
R2: 27kΩ
D1: 2.7V, 0.5W Zener Diode

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC_C}	-0.3	15	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (100 cd/m^2)		10,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC_C} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	C.I.E. 1931	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	C.I.E. 1931	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC_C} = 12.0V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{DD}		2.4	2.8	3.3	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	2.8	V_{DD}	V
Supply Voltage for Display	V_{CC_C}	Note 5	11.5	12.0	12.5	V
High Level Input	V_{IH}		0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}	I_{OH} = -0.1mA	V_{DD}-0.4	-		V
Low Level Output	V_{OL}	I_{OL} = -0.1mA		-	0.4	V
Operating Current for V_{DD}	I_{DD}		-	1.5	3.5	mA
Operating Current for V_{CC_C}	I_{CC_C}	Note 6	-	6.4	8.0	mA
		Note 7	-	9.5	12.0	mA
		Note 8	-	16.0	20.0	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	3	5	μA
Sleep Mode Current for V_{CC_C}	$I_{CC\_C, SLEEP}$		-	1	5	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC_C}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{CC_C} = 12.0V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC_C} = 12.0V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC_C} = 12.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

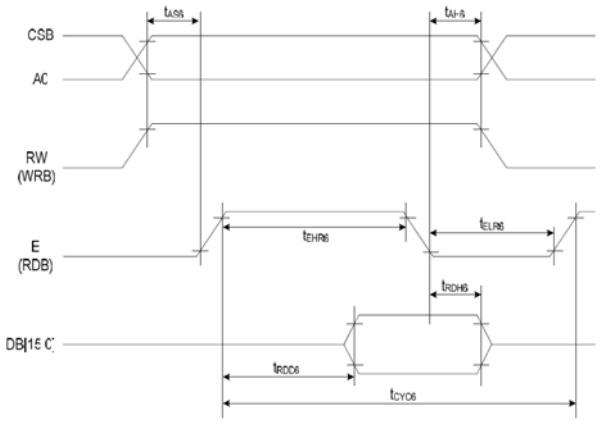
3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

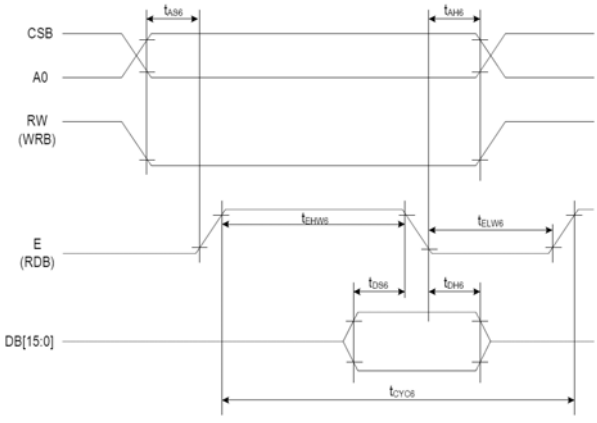
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description		Min	Max	Unit	Port
t_{AH6}	Address Setup Timing	(Read)	10	-	ns	CSB RS
		(Write)	5	-	ns	
t_{AS6}	Address Hold Timing	(Read)	10	-	ns	
		(Write)	5	-	ns	
t_{CYC6}	System Cycle Timing		200	-	ns	E
t_{ELR6}	Read "L" Pulse Width		90	-	ns	
t_{EHR6}	Read "H" Pulse Width		90	-	ns	
t_{CYC6}	System Cycle Timing		100	-	ns	
t_{ELW6}	Write "L" Pulse Width		45	-	ns	
t_{EHW6}	Write "H" Pulse Width		45	-	ns	
t_{RDD6}	Read Data Output Delay Time	* CL = 15pF	0	70	ns	D[7:0]
t_{RDH6}	Data Hold Timing		0	70	ns	
t_{DS6}	Data Setup Timing		40	-	ns	
t_{DH6}	Data Hold Timing		10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(***Read Timing***)



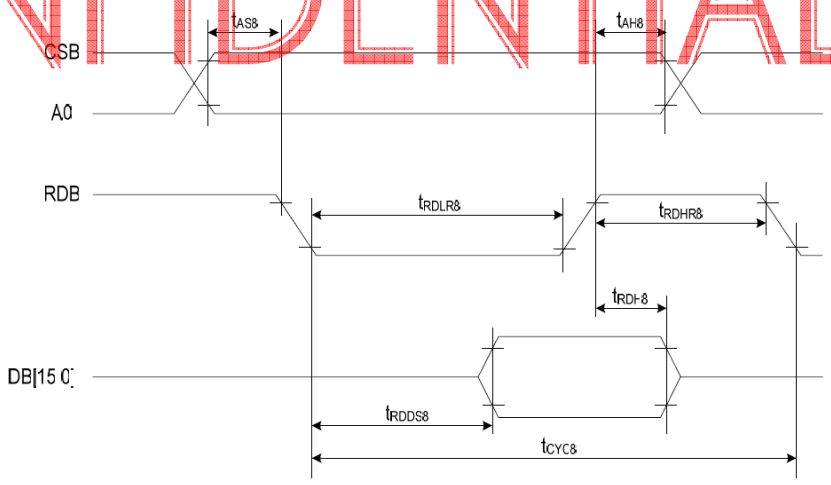
(***Write Timing***)

3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

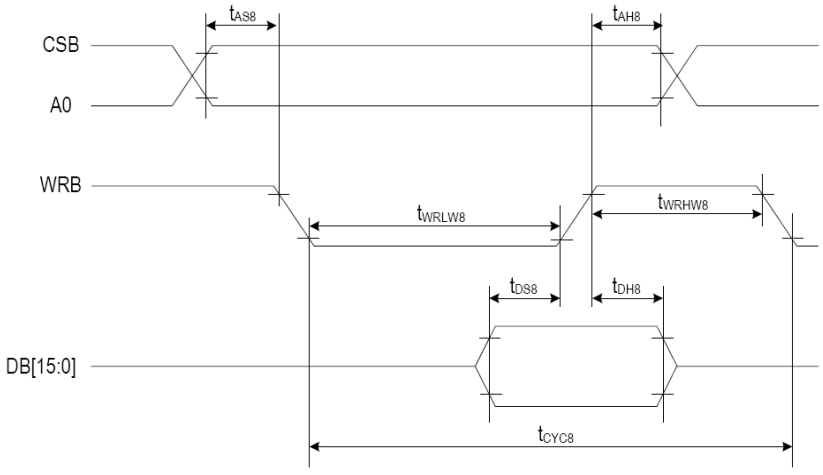
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{AS8}	Address Setup Timing	5	-	ns	CSB A0
t_{AH8}	Address Hold Timing	5	-	ns	
t_{CYC8}	System Cycle Timing	200	-	ns	RDB
t_{RDLR8}	Read "L" Pulse Width	90	-	ns	
t_{RDHR8}	Read "H" Pulse Width	90	-	ns	
t_{CYC8}	System Cycle Timing	100	-	ns	WRB
t_{WRLW8}	Write "L" Pulse Width	45	-	ns	
t_{WRHW8}	Write "H" Pulse Width	45	-	ns	
t_{RDD8}	Read Data Output Delay Time * CL = 15pF	-	60	ns	D[7:0]
t_{RDH8}	Data Hold Timing	0	60	ns	
t_{DS8}	Data Setup Timing	30	-	ns	
t_{DH8}	Data Hold Timing	10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(***Read Timing***)



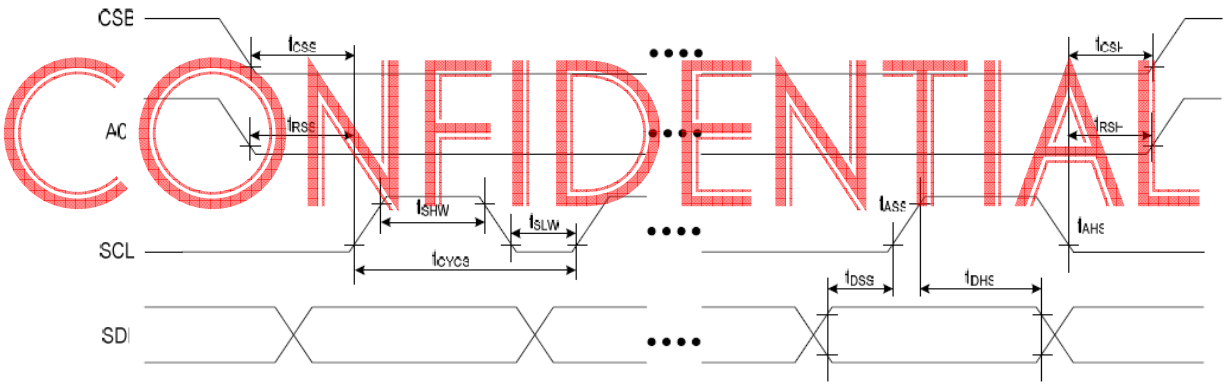
(***Write Timing***)

3.3.3 Serial Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{CYCS}	Serial Clock Cycle	200	-	ns	SCL
t_{SLW}	SCL "L" Pulse Width	90	-	ns	
t_{SHW}	SCL "H" Pulse Width	90	-	ns	
t_{DSS}	Data Setup Timing	25	-	ns	SDI
t_{DHS}	Data Hold Timing	25	-	ns	
t_{CSS}	CSB-SCL Timing	25	-	ns	CSB
t_{CSH}	CSB-Hold Timing	25	-	ns	
t_{RSS}	RS-SCL Timing	25	-	ns	A0
t_{RSH}	RS-Hold Timing	25	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



4. Functional Specification

4.1 Commands

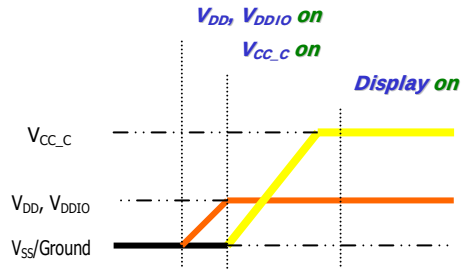
Refer to the Technical Manual for the SEPS114A

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

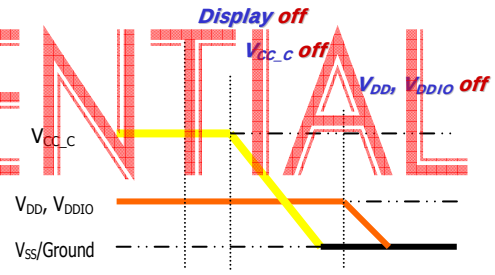
4.2.1 Power up Sequence:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC_C}
6. Delay 100ms
   (When V_{CC_C} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC_C}
3. Delay 100ms
   (When V_{CC_C} is reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



Note 8:

1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC_C} inside the driver IC, V_{CC_C} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{CC_C} is OFF.
2) V_{CC_C} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC_C}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{CC_C} power down.

4.3 Reset Circuit

When RSTB input is low, the chip is initialized with the following status:

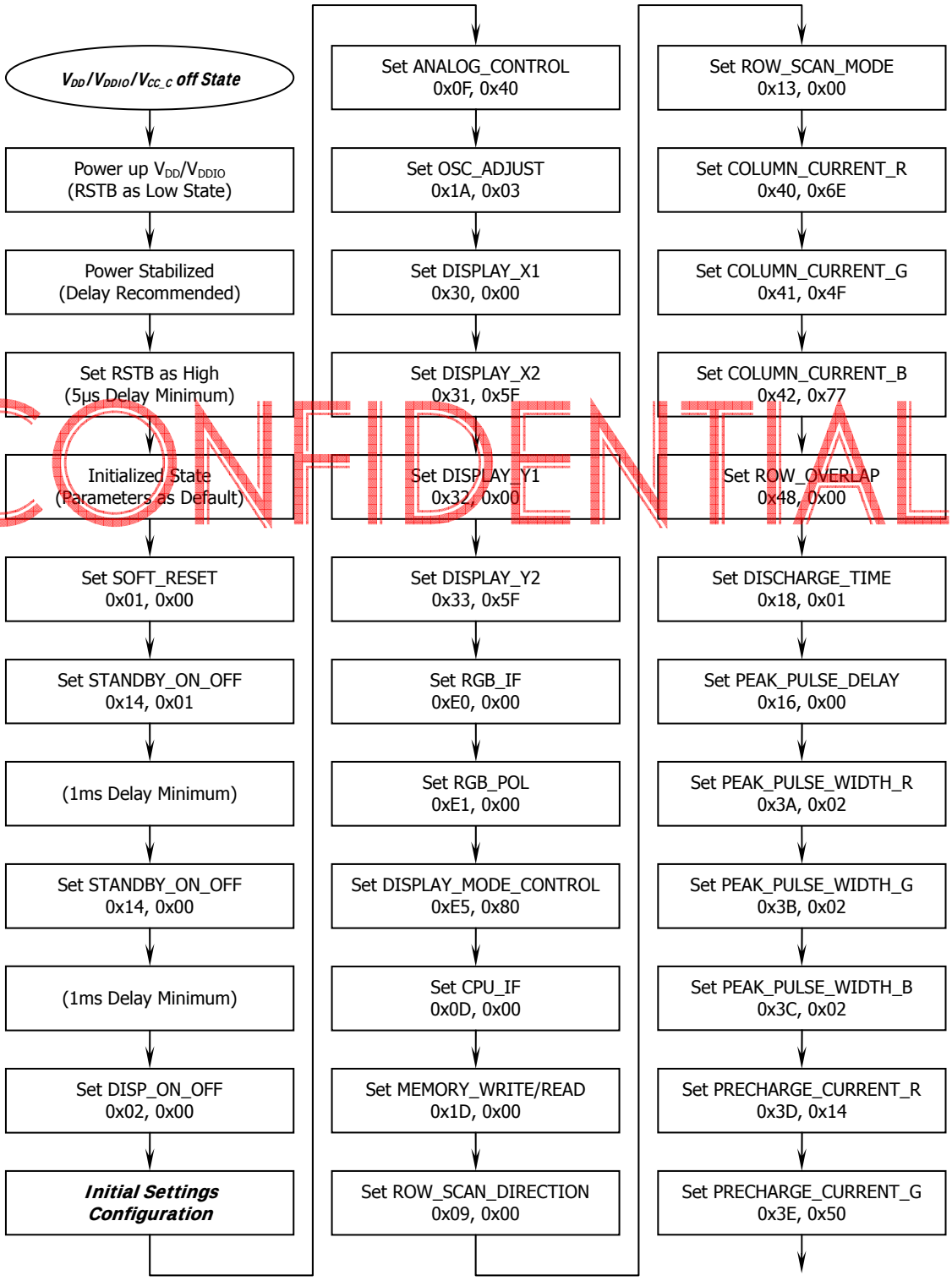
1. Standby Mode: On
2. Frame Frequency: 95Hz
3. Oscillation: Internal Oscillator Off
4. DDRAM Write Horizontal Address: XS = 0x00, XE = 0x5F
5. DDRAM Write Vertical Address: YS = 0x00, YE = 0x5F
6. Display Data RAM Write: MDIR1 = 0, MDIR0 = 0, VH = 0
7. Row Scan Shift Direction: R0, R1, … , R94, R95
8. Column Data Shift Direction: C0, C1, … , C286, C287
9. Display On/Off: Off
10. Panel Display Size: FX = 0x00, TX = 0x5F, FY = 0x00, TY = 0x5F
11. Display Data RAM Read Column/Row Address: DX = 0x00, DY = 0x00
12. Discharge Time: 8 Clock
13. Peak Pulse Delay: 5 Clock
14. Peak Pulse Width Time (R/G/B): 5 Clock
15. Precharge Current (R/G/B): 0μA

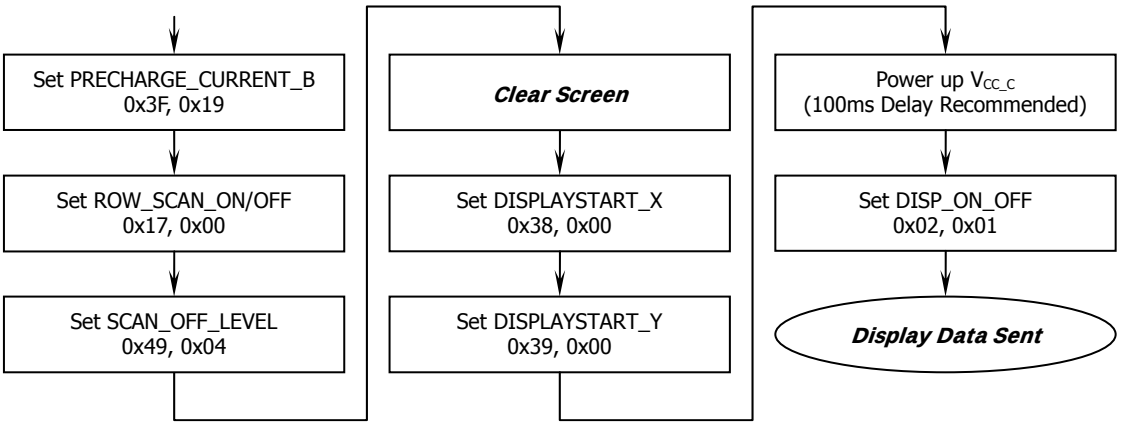
16. Driving Current (R/G/B): 0μA

4.4 Actual Application Example

Command usage and explanation of an actual example

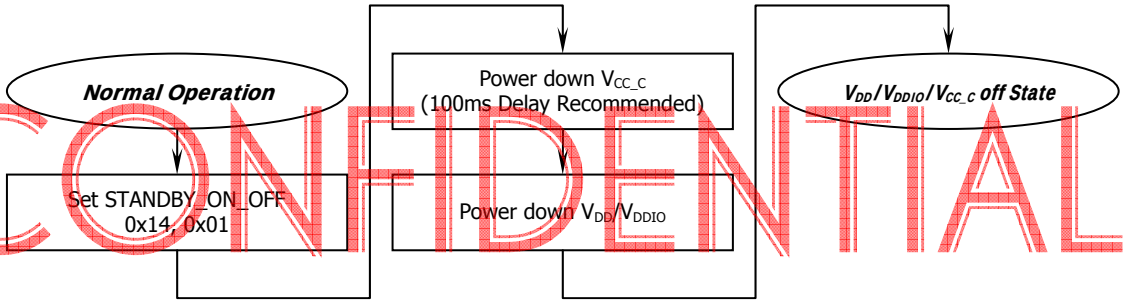
<Power up Sequence>



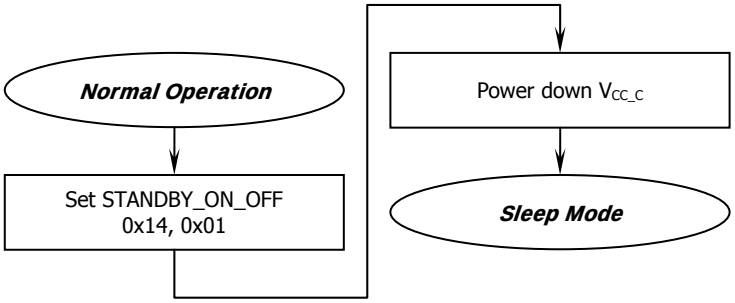


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>