

# Product Specification

(Preliminary)

Part Name: OEL Display Module

Customer Part ID:

WiseChip Part ID: UG-2832HLBEG04

Doc No.: SAS1-0B038-A

Customer:
Approved by

CONFIDENTIAL

From: WiseChip Semiconductor Inc.
Approved by

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### Notes:

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.



Revised History

Part Number	Revision	Revision Content	Revised on
UG-2832HLBEG04	A	New	March 1, 2011
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## 1. Basic Specifications

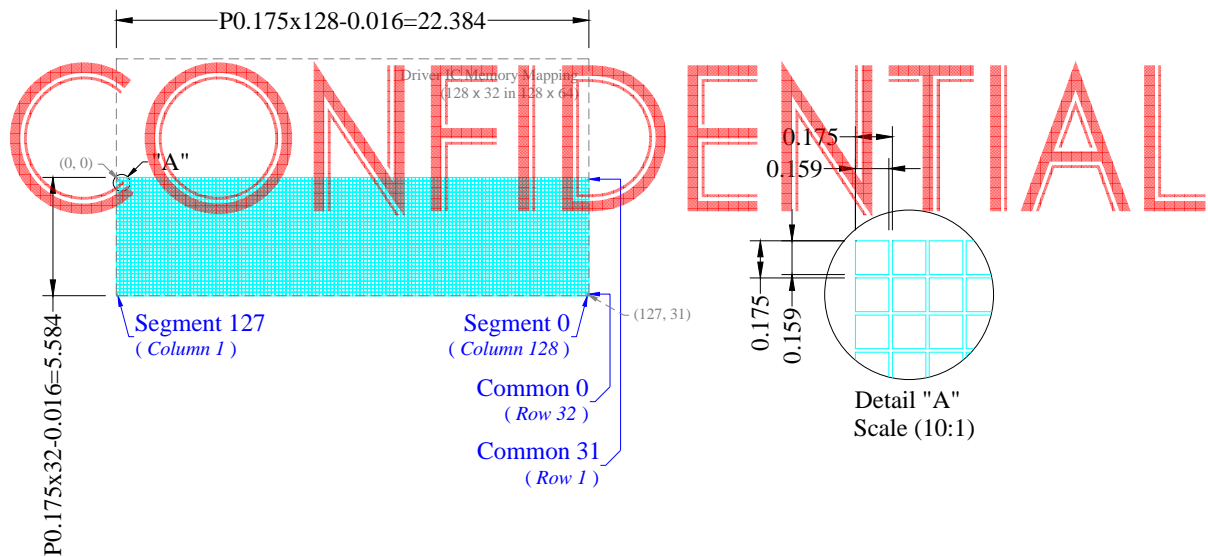
### 1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (Light Blue)
- 3) Drive Duty: 1/32 Duty

### 1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels: 128 × 32
- 3) Panel Size: 30.00 × 11.50 × 1.45 (mm)
- 4) Active Area: 22.384 × 5.584 (mm)
- 5) Pixel Pitch: 0.175 × 0.175 (mm)
- 6) Pixel Size: 0.159 × 0.159 (mm)
- 7) Weight: 1.05 (g)

### 1.3 Active Area / Memory Mapping & Pixel Construction



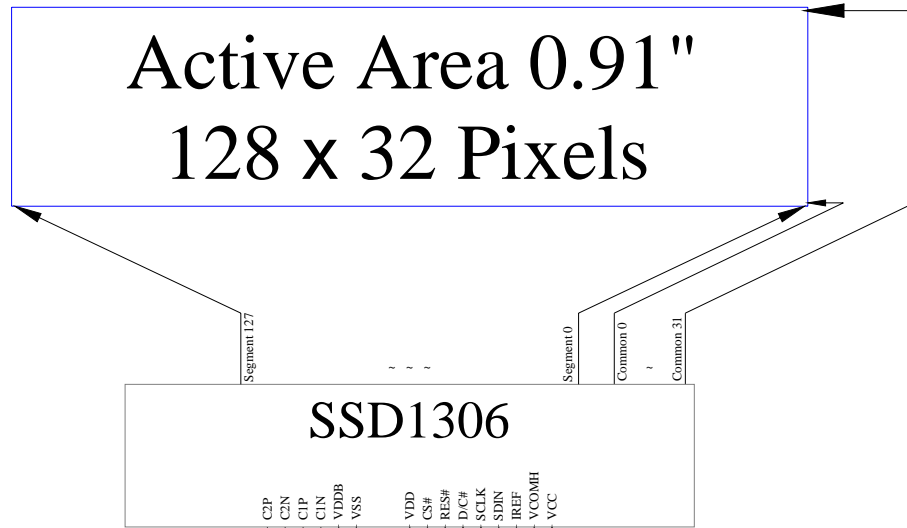


**1.5 Pin Definition**

Pin Number	Symbol	I/O	Function
<b>Power Supply</b>			
7	VDD	P	<b>Power Supply for Logic</b> This is a voltage supply pin. It must be connected to external source.
6	VSS	P	<b>Ground of OEL System</b> This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
15	VCC	P	<b>Power Supply for OEL Panel</b> This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V <sub>SS</sub> when the converter is used. It must be connected to external source when the converter is not used.
<b>Driver</b>			
13	IREF	I	<b>Current Reference for Brightness Adjustment</b> This pin is segment current reference pin. A resistor should be connected between this pin and V <sub>SS</sub> . Set the current at 12.5μA maximum.
14	VCOMH	O	<b>Voltage Output High Level for COM Signal</b> This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V <sub>SS</sub> .
<b>DC/DC Converter</b>			
5	VDDB	P	<b>Power Supply for DC/DC Converter Circuit</b> This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V <sub>SS</sub> when the converter is not used.
3 / 4 1 / 2	C1P / C1N C2P / C2N	I	<b>Positive Terminal of the Flying Inverting Capacitor</b> <b>Negative Terminal of the Flying Boost Capacitor</b> The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
<b>Interface</b>			
9	RES#	I	<b>Power Reset for Controller and Driver</b> This pin is reset signal input. When the pin is low, initialization of the chip is executed.
8	CS#	I	<b>Chip Select</b> This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
10	D/C#	I	<b>Data/Command Control</b> This pin is Data/Command control pin. When the pin is pulled high, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
11	SCLK	I	<b>Serial Clock Input Signal</b> The transmission of information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
12	SDIN	I	<b>Serial Data Input Signal</b> This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock. SDIN is identified to display data or command by D/C# bit data at the rising of first SCLK.

1.6 Block Diagram

1.6.1 V<sub>CC</sub> Supplied Externally

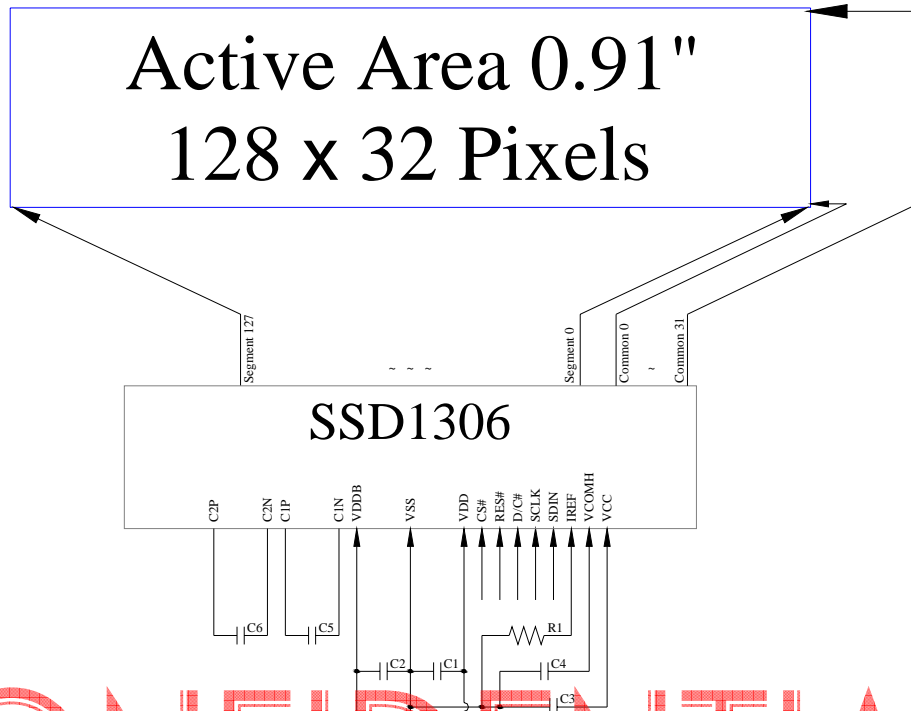


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Pins connected to MCU interface: RES#, SCL, and SDA

- C1: 1μF
- C2: 4.7μF
- C3: 4.7μF / 16V X7R
- R1: 390kΩ,  $R1 = (\text{Voltage at IREF} - VSS) / IREF$

1.6.2  $V_{CC}$  Generated by Internal DC/DC Circuit



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Pins connected to MCU interface: RES#, SCL, and SDA

- C1, C2: 1 $\mu$ F
- C3: 2.2 $\mu$ F
- C4: 4.7 $\mu$ F / 16V X7R
- C5, C6: 1 $\mu$ F / 16V X5R
- R1: 390k $\Omega$ ,  $R1 = (\text{Voltage at IREF} - VSS) / IREF$





2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V <sub>DD</sub>	-0.3	4	V	1, 2
Supply Voltage for Display	V <sub>CC</sub>	0	11	V	1, 2
<i>Supply Voltage for DC/DC</i>	<i>V<sub>DDB</sub></i>	<i>-0.3</i>	<i>5</i>	<i>V</i>	<i>1, 2</i>
Operating Temperature	T <sub>OP</sub>	-40	70	°C	
Storage Temperature	T <sub>STG</sub>	-40	85	°C	3
Life Time (120 cd/m <sup>2</sup> )		10,000	-	hour	4

Note 1: All the above voltages are on the basis of "V<sub>SS</sub> = 0V".

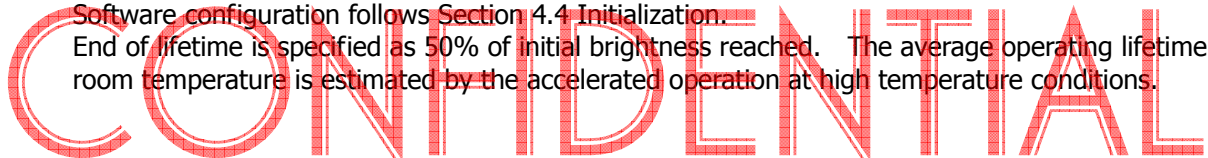
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V<sub>CC</sub> = 7.25V, T<sub>a</sub> = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.



### 3. Optics & Electrical Characteristics

#### 3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	$L_{br}$	Note 5	120	150	-	cd/m <sup>2</sup>
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

\* Optical measurement taken at  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ .  
Software configuration follows Section 4.4 Initialization.

#### 3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	$V_{DD}$		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	$V_{CC}$	Note 5 (Internal DC/DC Disable)	7.0	7.25	7.5	V
Supply Voltage for DC/DC	$V_{DDB}$	Internal DC/DC Enable	3.3	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	$V_{CC}$	Note 5 (Internal DC/DC Enable)	7.0	-	7.5	V
High Level Input	$V_{IH}$	$I_{OUT} = 100\mu A$ , 3.3MHz	$0.8 \times V_{DD}$	-	$V_{DD}$	V
Low Level Input	$V_{IL}$	$I_{OUT} = 100\mu A$ , 3.3MHz	0	-	$0.2 \times V_{DD}$	V
High Level Output	$V_{OH}$	$I_{OUT} = 100\mu A$ , 3.3MHz	$0.9 \times V_{DD}$	-	$V_{DD}$	V
Low Level Output	$V_{OL}$	$I_{OUT} = 100\mu A$ , 3.3MHz	0	-	$0.1 \times V_{DD}$	V
Operating Current for $V_{DD}$	$I_{DD}$		-	180	300	$\mu A$
Operating Current for $V_{CC}$ ( $V_{CC}$ Supplied Externally)	$I_{CC}$	Note 6	-	3.0	3.8	mA
		Note 7	-	4.5	5.6	mA
		Note 8	-	7.8	9.8	mA
Operating Current for $V_{DDB}$ ( $V_{CC}$ Generated by Internal DC/DC)	$I_{DDB}$	Note 6	-	9.1	11.4	mA
		Note 7	-	13.3	16.6	mA
		Note 8	-	21.7	27.1	mA
Sleep Mode Current for $V_{DD}$	$I_{DD, SLEEP}$		-	1	5	$\mu A$
Sleep Mode Current for $V_{CC}$	$I_{CC, SLEEP}$		-	2	10	$\mu A$

Note 5: Brightness ( $L_{br}$ ) and Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics and the customer's request.

Note 6:  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ , 30% Display Area Turn on.

Note 7:  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ , 50% Display Area Turn on.

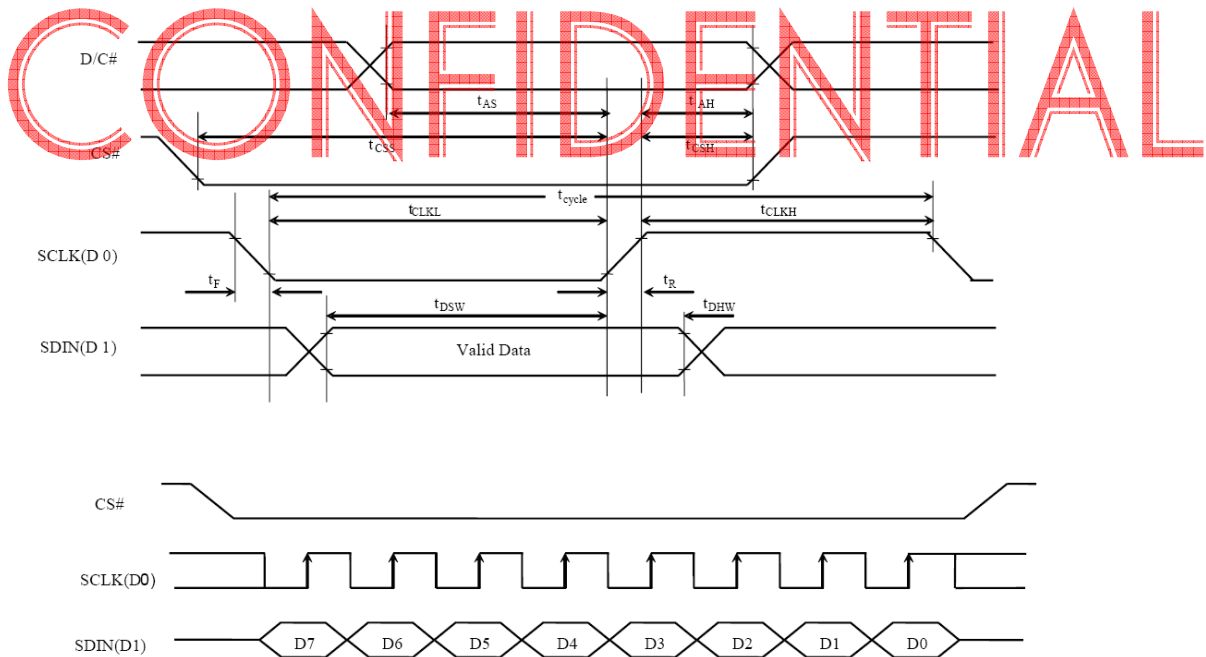
Note 8:  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ , 100% Display Area Turn on.

\* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

Symbol	Description	Min	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	ns
$t_{AS}$	Address Setup Time	15	-	ns
$t_{AH}$	Address Hold Time	15	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	ns
$t_{CSH}$	Chip Select Hold Time	10	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	ns
$t_{CLKL}$	Clock Low Time	20	-	ns
$t_{CLKH}$	Clock High Time	20	-	ns
$t_R$	Rise Time	-	40	ns
$t_F$	Fall Time	-	40	ns

\* ( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )



## 4. Functional Specification

### 4.1 Commands

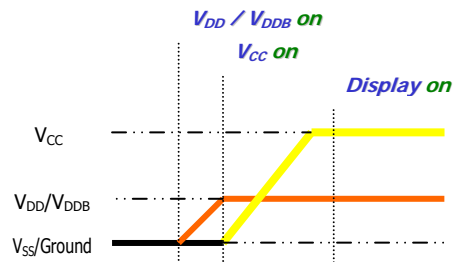
Refer to the Technical Manual for the SSD1306

### 4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

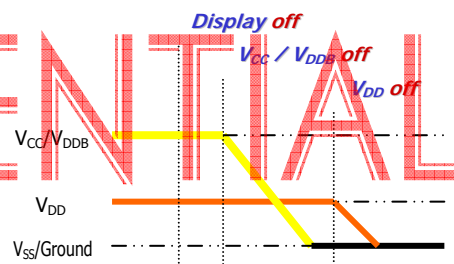
#### 4.2.1 Power up Sequence:

1. Power up  $V_{DD} / V_{DDB}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



#### 4.2.2 Power down Sequence:

1. Send Display off command
2. Power down  $V_{CC} / V_{DDB}$
3. Delay 100ms  
(When  $V_{CC} / V_{DDB}$  is reach 0 and panel is completely discharges)
4. Power down  $V_{DD}$



#### Note 9:

- 1) Since an ESD protection circuit is connected between  $V_{DD}$  and  $V_{CC}$  inside the driver IC,  $V_{CC}$  becomes lower than  $V_{DD}$  whenever  $V_{DD}$  is ON and  $V_{CC}$  is OFF.
- 2)  $V_{CC} / V_{DDB}$  should be kept float (disable) when it is OFF.
- 3) Power Pins ( $V_{DD}$ ,  $V_{CC}$ ,  $V_{DDB}$ ) can never be pulled to ground under any circumstance.
- 4)  $V_{DD}$  should not be power down before  $V_{CC} / V_{DDB}$  power down.

### 4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

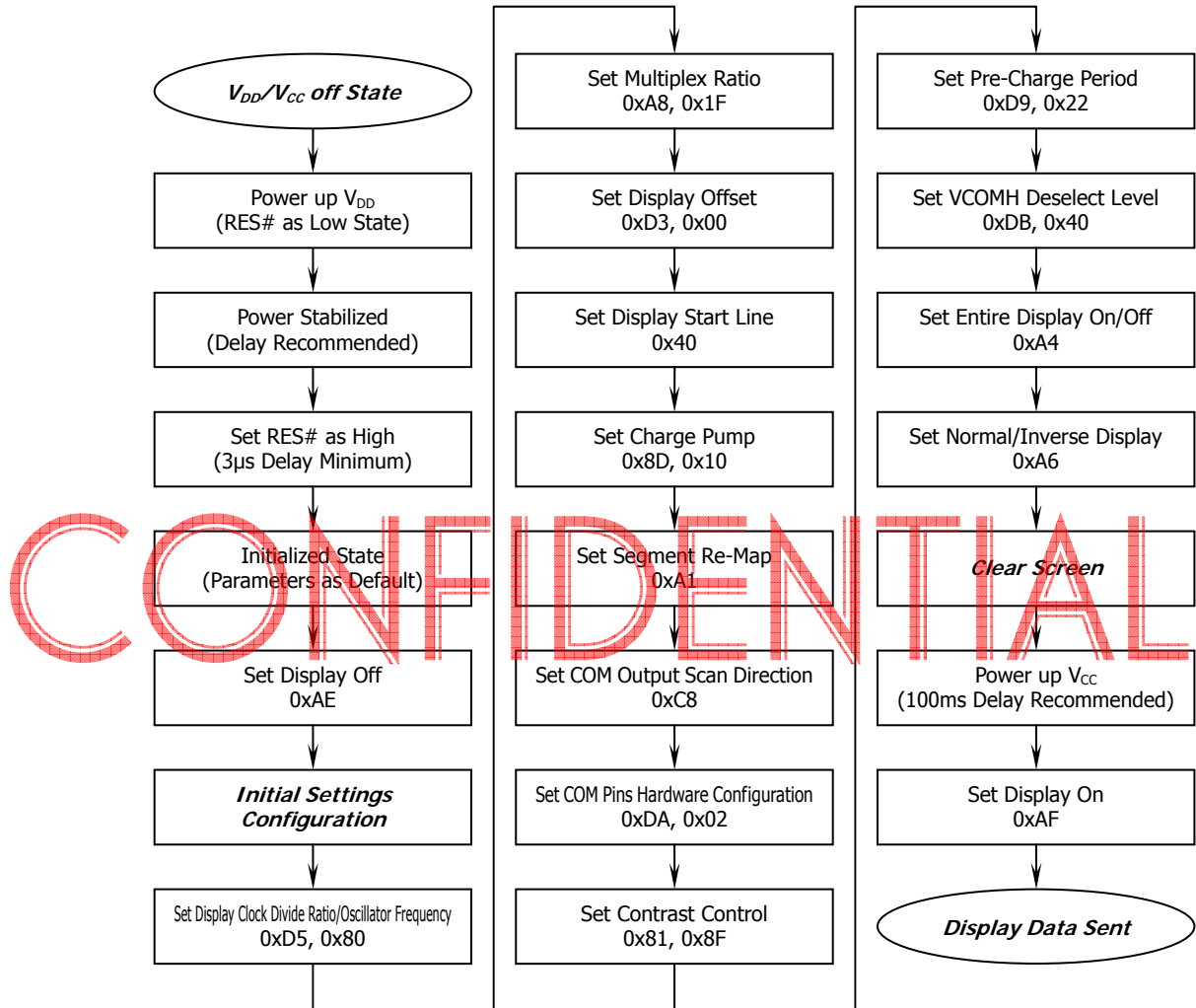
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

#### 4.4 Actual Application Example

Command usage and explanation of an actual example

##### 4.4.1 V<sub>CC</sub> Supplied Externally

<Power up Sequence>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

