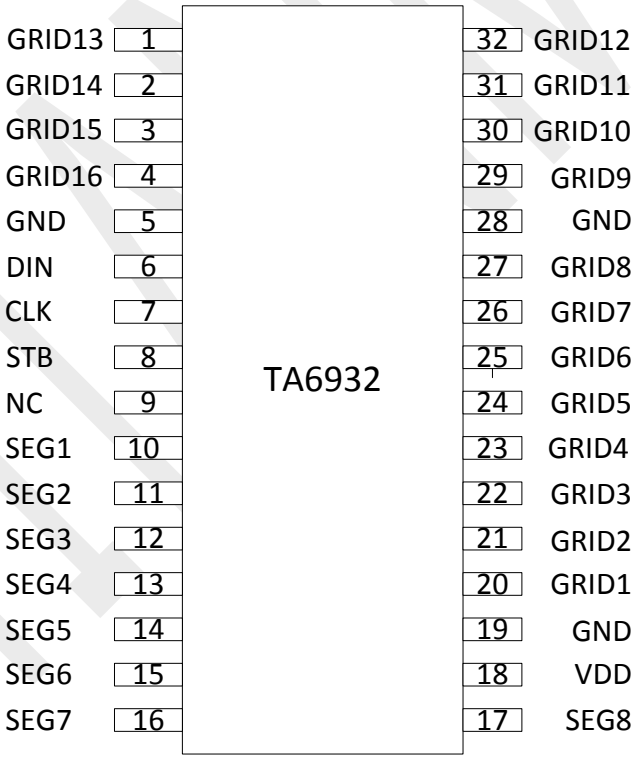
Overview

TA6932 is a special circuit for LED (light-emitting diode display) drive control. It integrates MCU digital interface, data latch and LED high-voltage drive. This product has excellent performance and reliable quality. It is mainly used in multi-segment display drive. It adopts SOP32 packaging mode.

Characteristics Description

- Adopt power CMOS process
- Display mode (8 segments × 16 bits)
- Brightness adjustment circuit (duty cycle is adjustable at 8 levels)
- Serial interface (CLK, STB, DIN)
- Oscillation mode: RC oscillation (450KHz + 5%)
- Built-in power-on reset circuit
- Packaging mode: SOP32

Pin Definition:



Pin Description

Symbol	Pin Name	Description
DIN	Data input	Serial data is input on the rising edge of the clock, starting from the low bit. It can be shorted to DOUT for use as DIO
STB	Chip selection	The serial interface is initialized on a rising or falling edge and then waits to receive an instruction. STB is the first byte after the low as the instruction. When the instruction is processed, the other processing is terminated. CLK is ignored when STB is high
CLK	Clock input	Input and output serial data on the rising edge of the clock
SEG1～SEG8	Output (segment)	Segment output, P tube open drain output
GRID1～GRID16	Output (bit)	Bit output, tube open drain output
VDD	Logic power supply	5V±10%
GND	Logically	System ground
NC	Empty pin	Internally unconnected

Figure (1)

Display the register address and display mode:

This register stores the data transferred from the external device to the TA6932 through the serial interface. The address is from 00H-0FH for a total of 16 bytes.
Corresponding to the LED lights connected to the SGE and GRID pins of the chip, the allocation is shown in following diagram:

When writing LED display data, it operates from the low to the high bit of the data byte, from the low to the high bit of the data byte.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	
xxHL (low level four bits)				xxHU (high level four bits)				
B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				GRID1
01HL				01HU				GRID2
02HL				02HU				GRID3
03HL				03HU				GRID4
04HL				04HU				GRID5
05HL				05HU				GRID6
06HL				06HU				GRID7
07HL				07HU				GRID8
08HL				08HU				GRID9
09HL				09HU				GRID10
0AHL				0AHU				GRID11
0BHL				0BHU				GRID12
0CHL				0CHU				GRID13
0DHL				0DHU				GRID14
0EHL				0EHU				GRID15
0FHL				0FHU				GRID16

Figure (2)

Instructions Description:

The instructions are used to set the display mode and the status of the LED driver.

The first byte entered by DIN after the falling edge of STB is used as an instruction. After decoding, take the highest B7, B6 two bits to distinguish different instructions.

b7	b6	Instruction
0	1	Data instruction setting
1	0	Display control instruction setting
1	1	Address instruction setting

If STB is set high during an instruction or data transmission, serial communication is initialized and the instruction or data being transferred is invalid.(The previously transmitted instruction or data remains valid).

1. Data instruction setting:

This instruction is used to set the data write and read. The B1 and B0 bits are not allowed to set 01 or 11.

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	Features	Description
0	1	For irrelevant item, fill in 0				0	0	Data read and write mode setting	Write data to display register
0	1				0			Address increase mode Setting	Automatic address increase
0	1				1				Fixed address
0	1			0				Test mode setting (internal use)	Common mode
0	1			1					Test mode

2. Address instruction setting:

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	Display address
1	1	For irrelevant item, fill in 0		0	0	0	0	00h
1	1			0	0	0	1	01h
1	1			0	0	1	0	02h
1	1			0	0	1	1	03h
1	1			0	1	0	0	04h
1	1			0	1	0	1	05h
1	1			0	1	1	0	06h
1	1			0	1	1	1	07h
1	1			1	0	0	0	08h
1	1			1	0	0	1	09h
1	1			1	0	1	0	0Ah
1	1			1	0	1	1	0Bh
1	1			1	1	0	0	0Ch
1	1			1	1	0	1	0Dh
1	1			1	1	1	0	0Eh
1	1			1	1	1	1	0Fh

Figure (3)

This instruction is used to set the address of the display register.

If the address is set to 10H or higher, the data is ignored until the effective address is set.When powering up, the address is set to 00H by default.

3. Display control:

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	Features	Description
1	0	For irrelevant item, fill in 0			0	0	0	Extinction quantity setting	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch setting	Display OFF
1	0			1					Display ON

Figure (4)

Serial Data Transmission Format:

Data reception (write data)

Receive rising edge operation with 1 BIT at the clock.

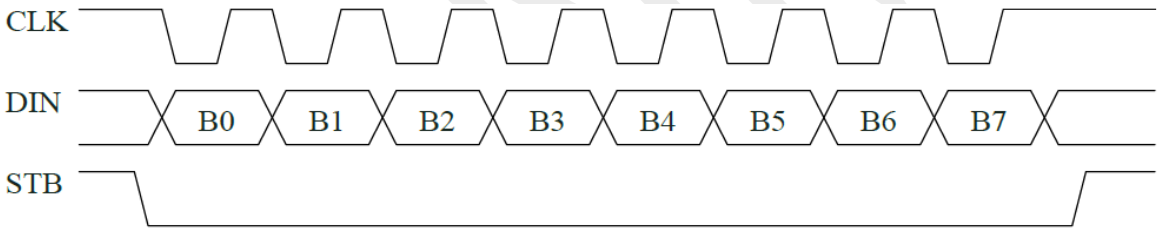


Figure (5)

▲**Note**: When reading data, one waiting time Twait (minimum 1μS) is necessary from the 8th rising edge of the serial clock CLK
to the falling edge of CLK.

Display:

1.Drive the common cathode digital tube:

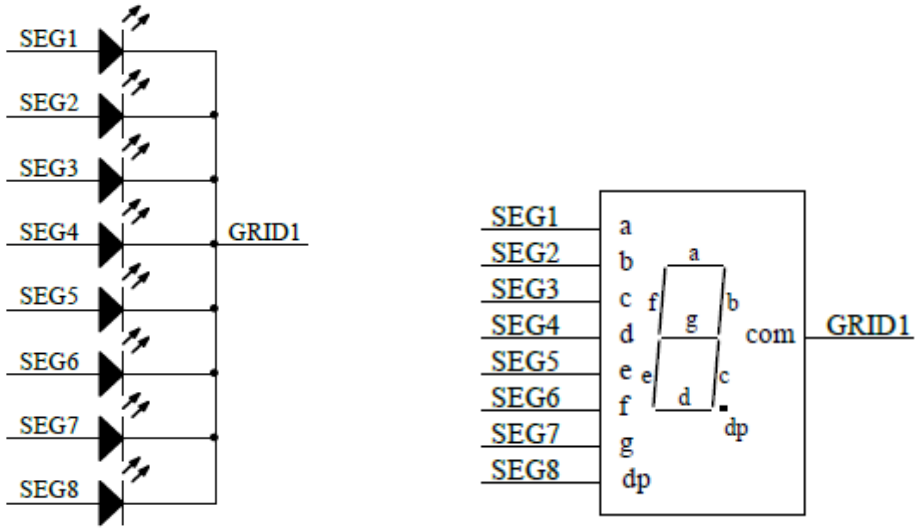


Image (6)

Figure (6) shows the connection diagram of the common cathode digital tube. If the digital tube is displayed as "0", then you need to set SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 at high level, SEG7 at low level be low when GRID1 is at low level, see Figure (2) to display the address table. Simply write the data 3FH in the 00H address unit to make the digital tube display "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

2.Drive the common Yang digital tube :

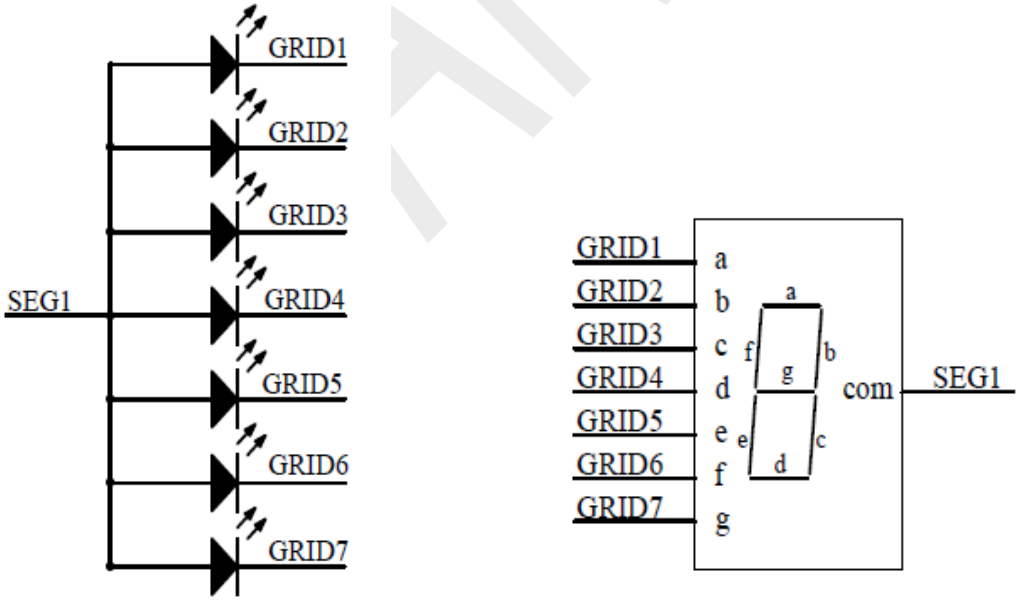


Figure (7)

Figure (7) shows the connection diagram of the common digital tube. If the digital tube is displayed as "0", then you need to set SEG1 GRID1, GRID2, when GRID1, GRID3, GRID4, GRID5 and GRID6 at low level, when GRID7 is at low level. To write data 01H to address unit 00H-05H, all the remaining address units write 00H.

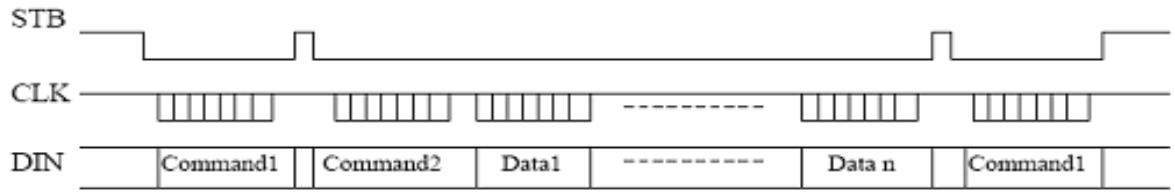
SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	00h
0	0	0	0	0	0	0	1	01h
0	0	0	0	0	0	0	1	02h
0	0	0	0	0	0	0	1	03h
0	0	0	0	0	0	0	1	04h
0	0	0	0	0	0	0	1	05h
0	0	0	0	0	0	0	0	06h
b7	b6	b5	b4	b3	b2	b1	b0	

▲**Note**: SEG1-8 is the open drain output of P tube, GRID1-16 is the open drain output of N tube. In use, SEG can only connect the anode of LED, GRID
can only be connected to the cathode of the LED, can not be reversed.

Transmission of Serial Data during Application:

1. Mode of address automatically adding one

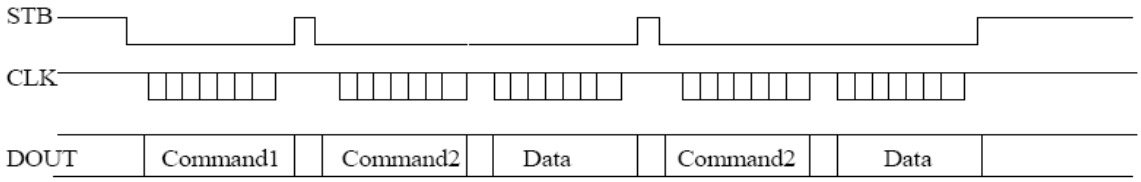
Use the mode of address automatically adding one, set the address is actually to set the starting address of saving the data stream to be transmitted. After sending the start address instrument word "STB" does not need to be set high to follow the data, up to 16BYTE, and "STB" is set high after the data transfer is completed.



Command1: Set data command
Command2: Set display address
Data1～ n: Transmit the display data to Command2 address and subsequent addresses (up to 16 bytes)
Command3: Display control command

2. Fixed address mode

Use the fixed address mode, set the address is actually to set the address of saving 1BYTE data to be transmitted. After transmitting the address."STB" does not need to be set high, followed by the 1BYTE data, and the "STB" is set high after transmitting the data. Then reset the address of saving the second data, up to 16BYTE data transfer is completed, "STB" is set high.



Command1: Set data command
Command2: Set display address 1
Data1: Transmit display data 1 to Command2 address
Command3: Set display address 2
Data2: Transmit display data 2 to Command3 address
Command4: Display control command

3. Program design flow chart:

Program flow chart with automatic address adding one:

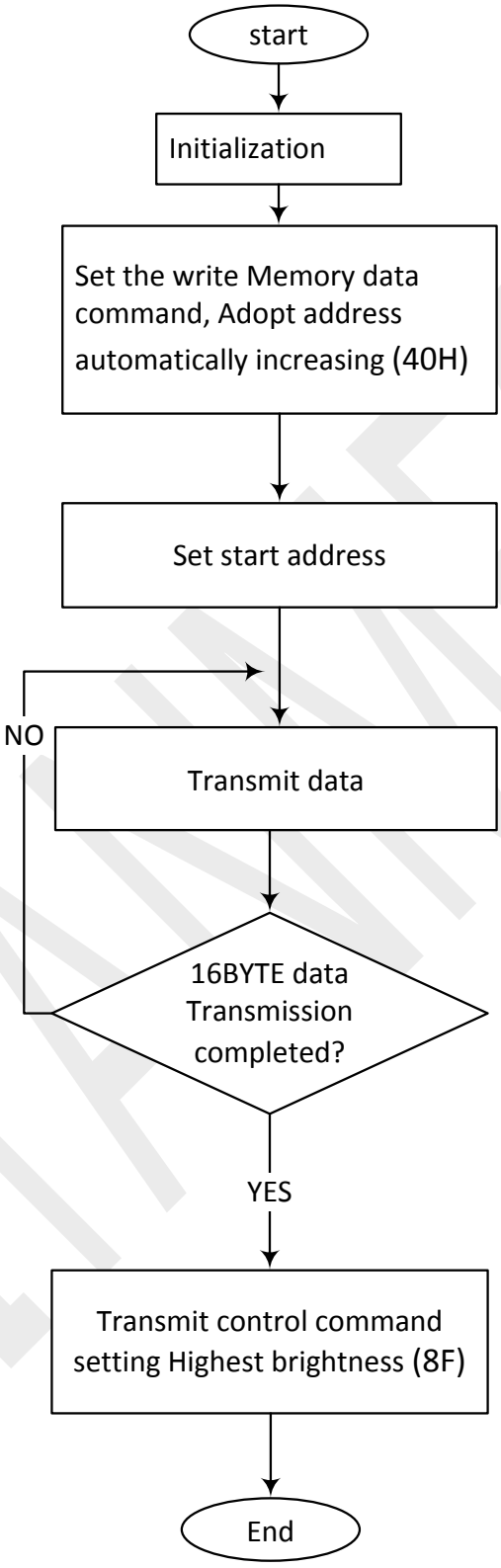


Figure (8)

Program design flow chart adopting fixed address:

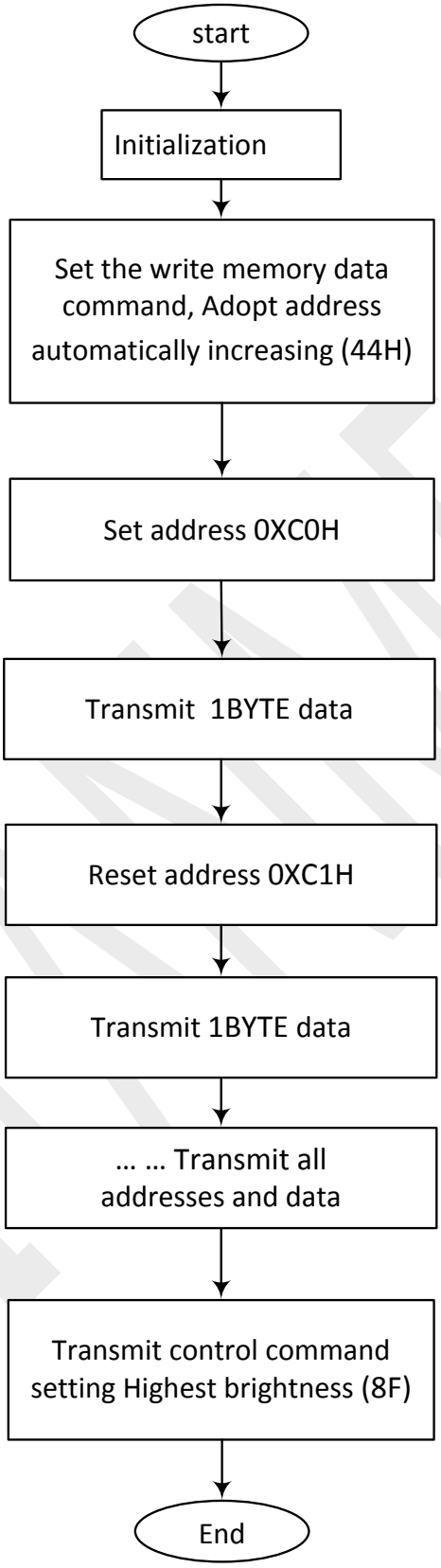


Figure (9)

Application Circuit:

1. TA6932 drive common Yin digital screen wiring circuit diagram (10):

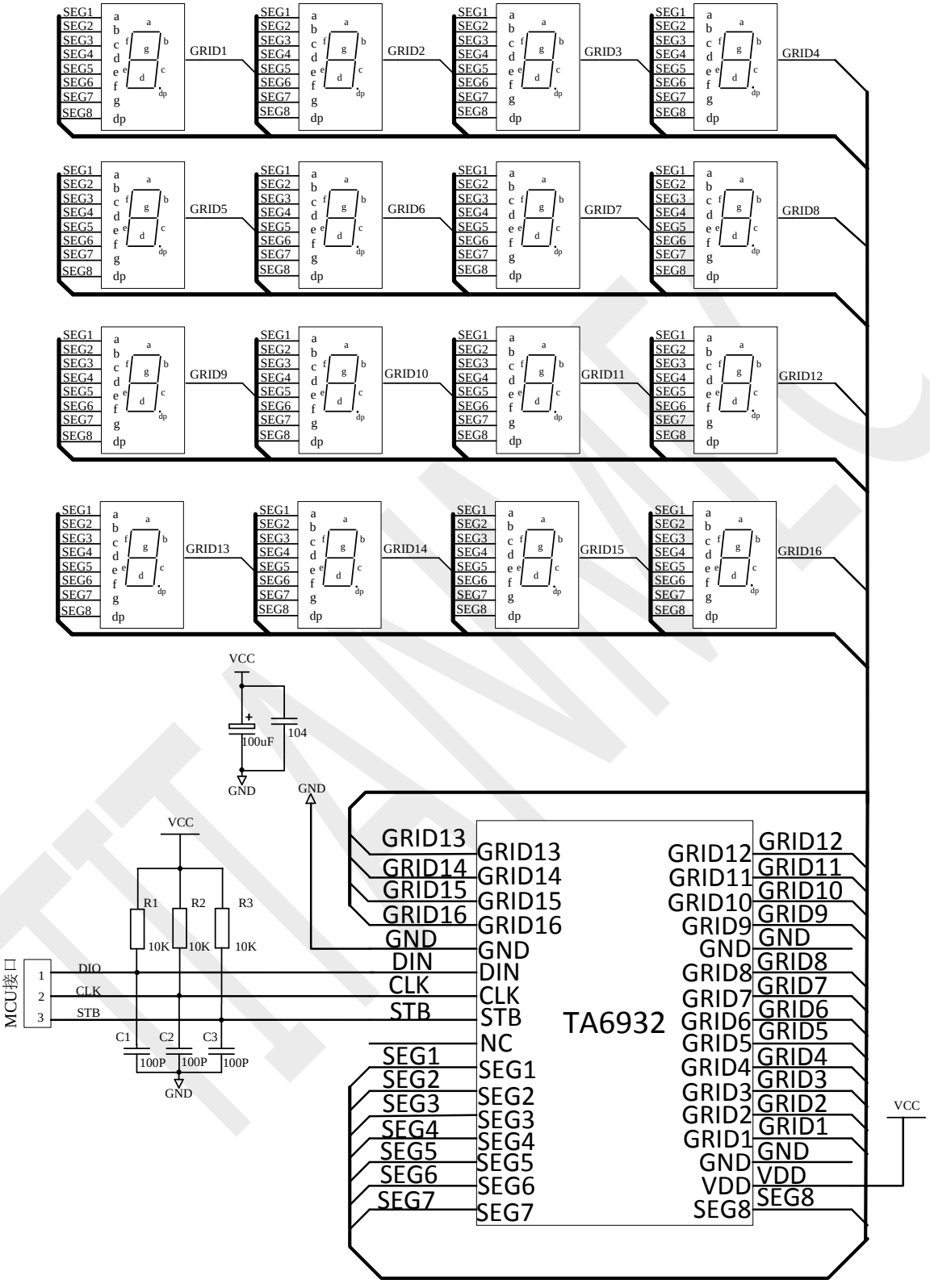


Figure (10)

2. TA6932 drive common positive pole digital screen wiring circuit diagram (11):

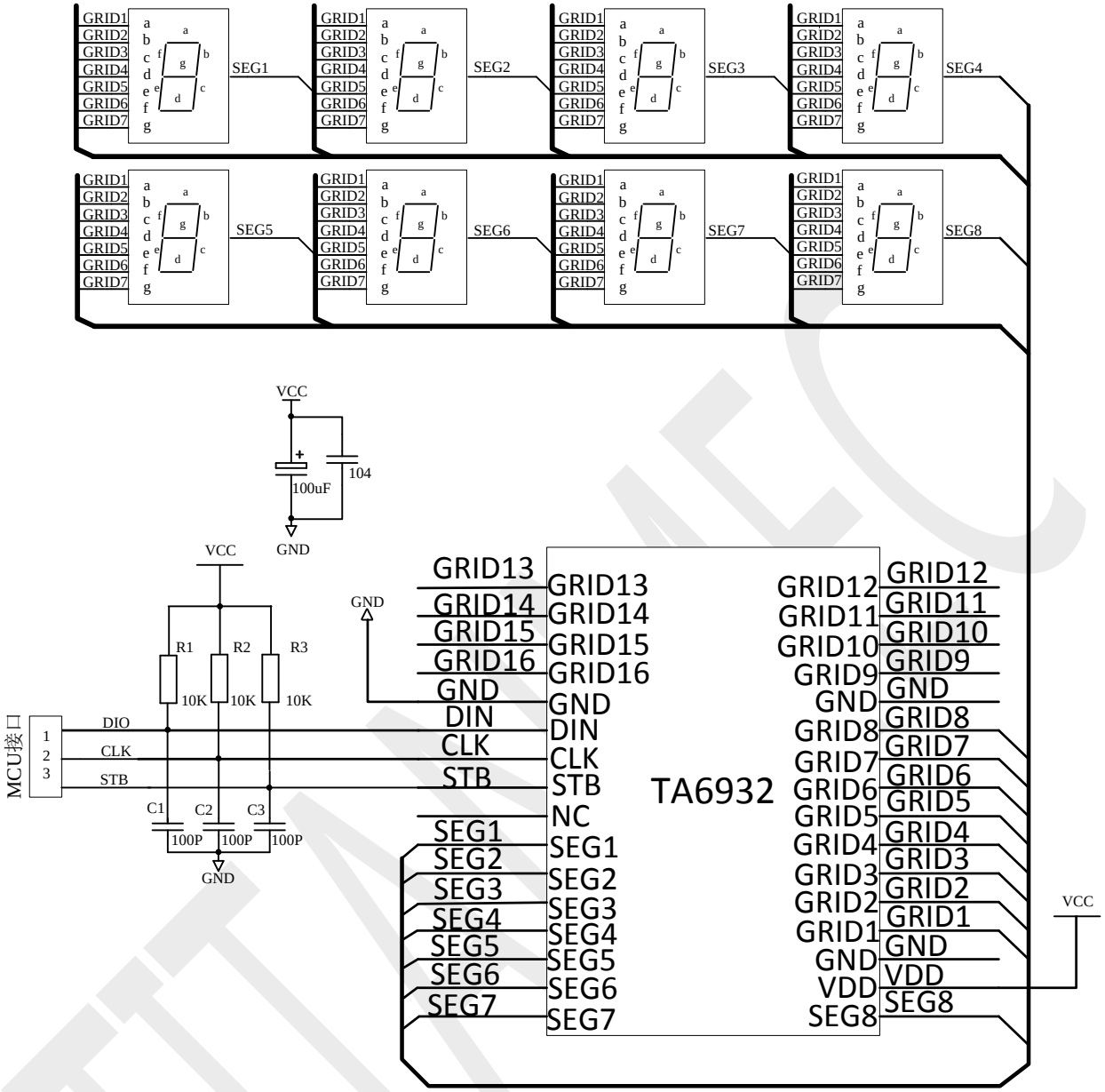


Figure (11)

▲Note: 1. The filter capacitor between VDD and GND should be placed on the PCB board as close as possible to the TA6932 chip to enhance the filtering effect.

2. Three 100P capacitors connected to the DIO, CLK, and STB communication ports can reduce the interference to the communication port.

3. Because the on-voltage of the blue digital tube is about 3V, the power supply of the TA6932 should be 5V.

Electrical Parameters:

Limit parameters (Ta = 25 ℃, Vss = 0 V)

Parameter	Symbol	Range	Unit
Logic Supply Voltage	V	-0.5~+7.0	V
Logic input voltage	VI1	0.5 W/VDD + 0.5 W/V	V
LED Seg drive output current	IO1	-50	mA
LED Grid drive output current	IO2	+200	mA
Power loss	PD	400	mW
Operating temperature	Topt	-40～ +80	°C
Storage temperature	Tstg	-65～+150	°C

Normal operating range (Ta = -20 ～ +70 ℃， Vss = 0 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions
Logic Supply Voltage	VDD	3	5	5.5	V	-
High level input voltage	Vih	0.7VDD	-	V	V	-
Low level input voltage	Vil	0	-	0.3Vdd	V	-

Electrical characteristics (Ta = -20 ～ +70 ℃,VDD = 4.5 ～ 5.5 V, Vss = 0 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions
High level output current	Ioh1	-20	-25	-40	mA	Seg1~Seg8, Vo=vdd-2.2V
	Ioh2	-20	-30	-50	mA	Seg1~Seg8, Vo=vdd-3.3V
Low level output current	IOL1	80	140	-	mA	Grid1~Grid16 Vo=0.3V
Low level output current	Idout	4	-	-	mA	VO=0.4V, dout
High level output current allowance	Itolsg	-	-	5	%	VO = VDD – 3V, Seg1～Seg
Output pull-down resistance	RL		10		KΩ	
Input current	II	-	-	±1	μA	VI = VDD / VSS
High level input voltage	Vih	0.7 VDD	-		V	CLK, DIN, STB
Low level input voltage	Vil	-	-	0.3 VDD	V	CLK, DIN, ST
Hysteresis voltage	VH	-	0.35	-	V	CLK, DIN, STB
Dynamic current loss	IDDdyn	-	-	5	mA	No load, display off

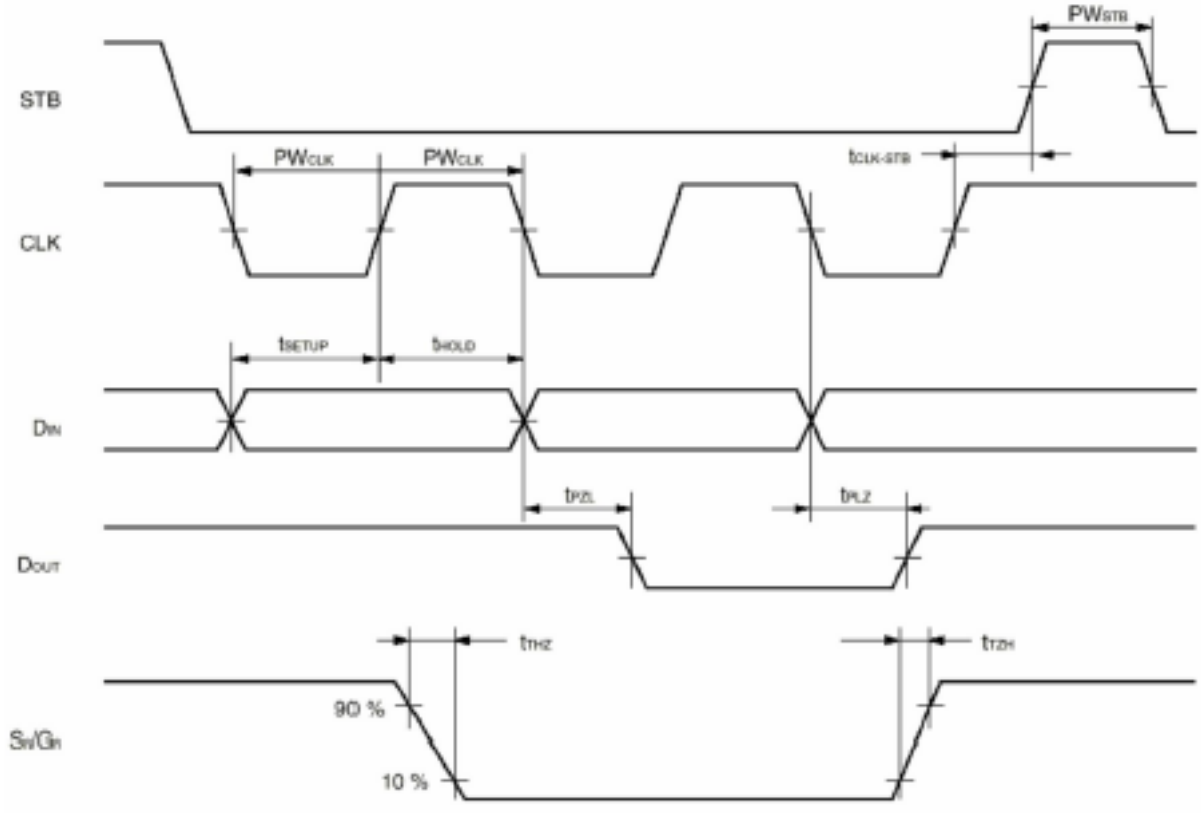
Switching characteristics (Ta = -20 ～ +70 ℃, VDD = 4.5 ～ 5.5 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions	
Oscillating frequency	fosc	-	500	-	KHz	R=16.5KΩ	
Transmission delay time	tPLZ	-	-	3	ns	CLK→ DOUT	
	tPZL	-	-	100	ns	CL=15pF, RL=10KΩ	
Rise time	TTZH1	-	-	2	μs	CL= 300p F	SEG1～SEG8
	TTZH 2	-	-	0.5	μs		GRID1～GRID16
Fall time	TTHZ	-	-	120	μs	CL=300pF, Segn, Gridn	
Maximum clock frequency	Δf maximum	1	-	-	MHZ	Duty cycle 50%	
Input capacitance	CI	-	-	15	pF	-	

Time sequence characteristics (Ta = -20 ～ +70 ℃, VDD = 4.5 ～ 5.5 V)

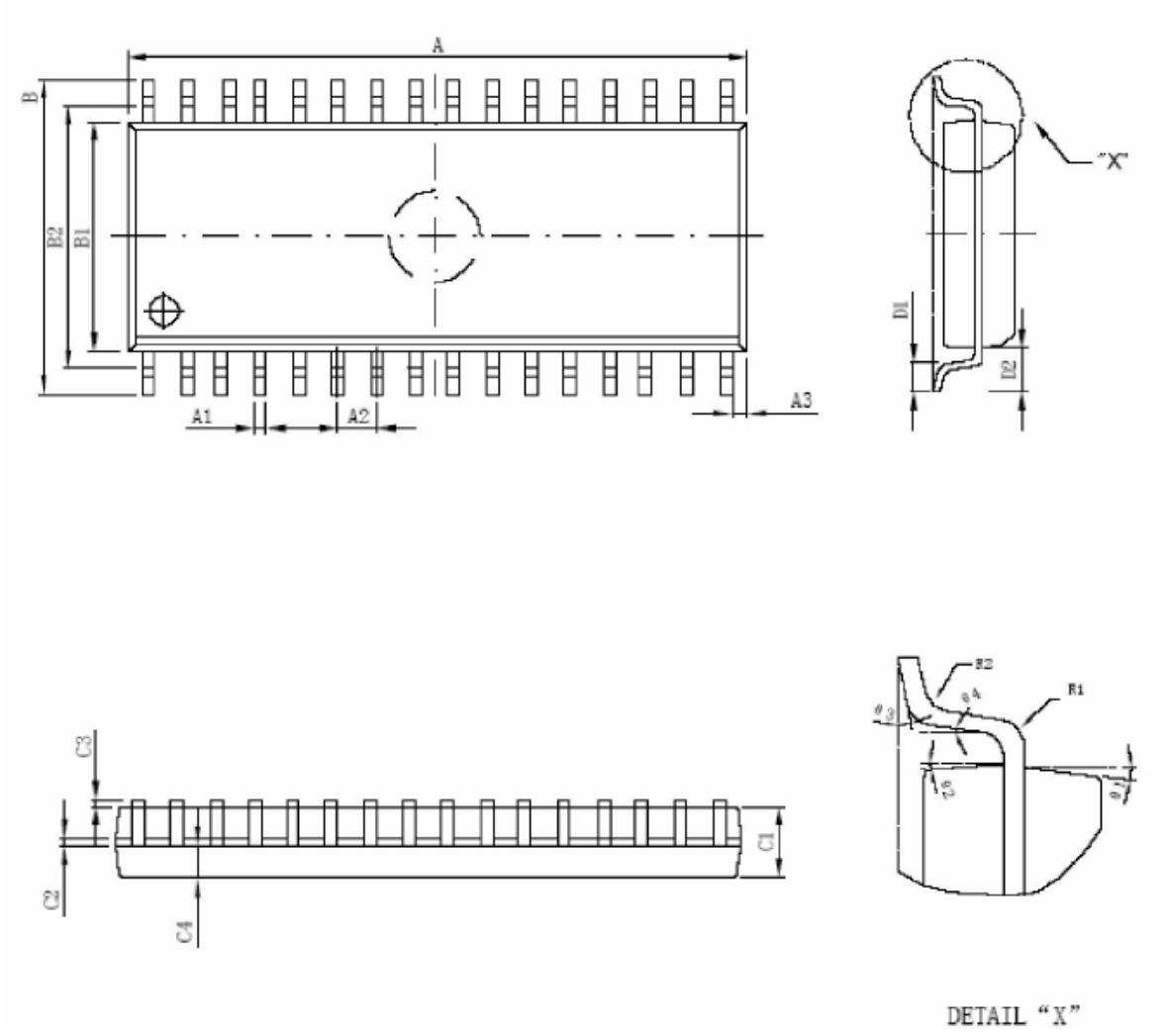
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions
Clock pulse width	PWCLK	400	-	-	ns	-
Gating pulse width					μs	-
Data establishment time					ns	-
Data hold time					ns	-
CLK → STB time					μs	CLK↑→STB↑
Waiting time					μs	CLK↑→CLK↓

Time sequence waveform diagram:



Packaging size

Mark / Size	Min(mm)	Max(mm)	Mark / Size	Min(mm)	Max(mm)
A	20.88	21.08	C4	0.99TYP	
A1	0.3	0.5	D1	0.55	0.95
A2	1.27TYP		D2	1.45	
A3	0.77TYP		R1		
B	10.2	10.6	R2		
B1	7.42	7.62	θ1	8° TYP	
B2	8.9TYP		θ2	15° TYP	
C1	2.14	2.34	θ3	4° TYP	
C2	0.2	0.32	θ4	14° TYP	
C3	0.10	0.25			



All specs and applications shown above subject to change without prior notice.

The last update date of this application document is: 2011-10-19