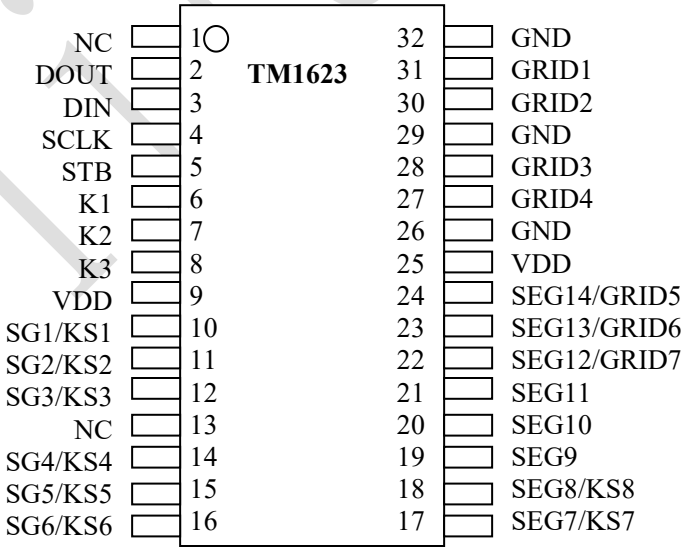
I. Introduction

TM1623 is an IC dedicated to LED (light emitting diode display) drive control. It integrates MCU digital interface, data latch, LED drive, and other circuits. This product is reliable in quality, stable in performance and strong in interference resistance. It is mainly used for household electrical appliances (smart water heaters, microwave ovens, washing machines, air conditioners, and electric stove), set-top boxes, electronic scale, smart meters and other other digital tube or LED display devices.

II. Features

- • Low power consumption CMOS workmanship
- Multiple display mode(11 Segments x 7 Grids ～14 Segments x 4 Grids)
- Key Scanning (10 x 3 Matrix)
- Luminance adjustment circuit (8-level adjustable duty cycle)
- Serial port (DIO,CLK,STB)
- Oscillation mode: built-in RC oscillation
- Built-in power-on reset circuit
- Data latch circuit in internal design
- Strong anti-interference ability
- Packaging:SOP32

III. Pin definition:



IV. Definition of pin function

Symbol	Pin Name	Pin ID	Description
DOUT	Data Output	2	Data Input Output Pin，(N-Channel , Open-Drain) This pin outputs serial data at the falling edge of the shift clock. Built-in 13.3K Ω pull-up resistor
DIN	Data Input	3	Input serial data at rising edge of the clock, starting from lower bits.
CLK	Clock input	4	Read serial data at rising edge and output data at falling edge. Built-in 13.3KΩ pull-up resistor
STB	Chip selection input	5	Initialize the serial interface at falling edge, then wait to receive instructions. The first byte after STB becomes low is considered as an instruction. When an instruction is being processed, other current processes are terminated. When S TB is high, CLK is ignored. Built-in 13.3KΩ pull-up resistor
K1-K3	Input	6-8	Key Data Input Pins，The data sent to these pins are latched at the end of the display cycle.(Internal Pull-Low Resistor)
SGE1～SEG11	Output (segment)	10-12 14-21	Segment output. This is a PMOS open drain output with a 4KΩ pull-down resistor
GRID1～ GRID4	Output (bit)	27～28 30～31	Bit output. This is a NMOS open drain output with a 2.7KΩ pull-up resistor
SEG12/DRID7 ～ SEG14/GRID5	Output (segment/bit)	22～24	Multiplexed output of either segment or bit
VDD	Logic Supply	9、25	Power +
GND	Logic GND	26、29、32	System GND

V. Description of Instructions

This instruction is used to set the display mode and the status of LED drive.

The first byte input by DIN after the falling edge of STB is considered as an instruction. After decoding, obtain the topmost B7 and B6 bits to distinguish different instructions.

B7	B6	Instruction
0	0	Setting of Display Mode Command
0	1	Setting of Data Command
1	0	Setting of Display Control Command
1	1	Setting of Address Command

If STB is set high during instruction or data transmission, serial communication is initialized, and the instruction or data being transmitted is invalid (but the instruction or data transmitted before remains active.)

（1） Setting of Display Mode Command:

This instruction is used to set the number of selectable segments and bits (4~7 bits, 11~14 segments) Display is forced off when this instruction is being executed. While the display mode remains unchanged, the data in the display memory will not be changed. The display control commend controls the ON and OFF of display. When powered on, the display mode by default is 7 bits×11 segments.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display mode
0	0	Unrelated item. Leave it to be 0				0	0	4 bits, 14 segments
0	0					0	1	5 bits, 13 segments
0	0					1	0	6 bits, 12 segments
0	0					1	1	7 bits, 11 segments

（2） Setting of Data Command:

This instruction is used to set data writing and reading. Bits B1 and B0 cannot set to 01 or 11.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	Unrelated item. Leave it to be 0				0	0	Setting of data read-write mode	Write data to the display register
0	1					1	0		Read key scanning data
0	1				0			Sett address increment mode	Auto increment
0	1				1				Fixed address
0	1			0				Test mode setting (for internal use)	Normal mode
0	1			1					Test mode

（3） Setting of Display Control Command:

This instruction is used to set the ON/OFF and brightness of display. A total of 8 levels of luminance are offered for adjustment.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	Unrelated item. Leave it to be 0			0	0	0	Setting of display luminance	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Setting of display switch	Display Off
1	0			1					Display ON

（4） Setting of Address Command：

This instruction is used to set the address of the display register. In the maximum case, there are 14 valid addresses (00H-0DH). If the address is OEH or higher, data will be ignored until a valid address is set. On power-up, the address is set to 00H by default.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	Unrelated item. Leave it to be 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH

VI. Address of display register:

The register stores data transmitted through the serial interface from an external device to TM1623, or, at valid addresses of 14 bytes ranging from 00H-0DH in the maximum case, each corresponding to the Chip SEG and GRID pins, as assigned below:
LED display data are written in an ascending order of both display address and data byte.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	X	X	
xxHL (low four)				xxHU (high four)				xxHL (low four)				xxHU (high four)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				**GRID1**
02HL				02HU				03HL				03HU				**GRID2**
04HL				04HU				05HL				05HU				**GRID3**
06HL				06HU				07HL				07HU				**GRID4**
08HL				08HU				09HL				09HU				**GRID5**
0AHL				0AHU				0BHL				0BHU				**GRID6**
0CHL				0CHU				0DHL				0DHU				**GRID7**

Figure (2)

▲ Note: The moment the display register of the chip is powered on, the values stored inside may be random, at which point, user may directly send a command to turn on the screen, and messy codes are likely to appear. Considering that, the company advise customers to clear the display register upon power-on, i.e., writing 0x00 into all the 14-byte memory addresses (00H-0DH).

VII. Display:

1. Driving common cathode LEDs:

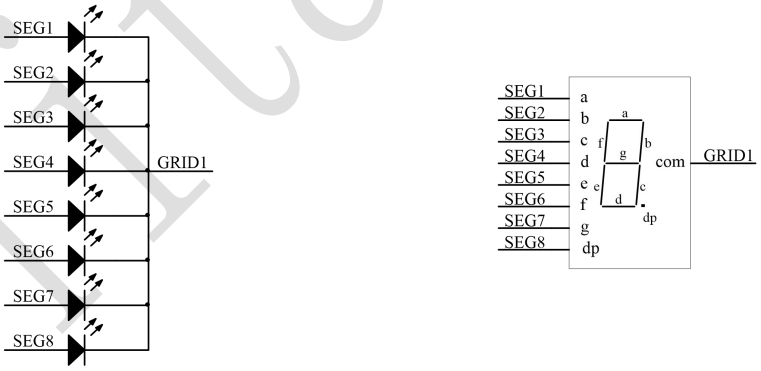


Figure (7)

Figure 7 is a diagram for the wiring of common cathode LEDs. To display 0 off the LED segment display, customers only need to write 0x3F to the 00H (GRID1) address starting from lower bits, at which point, 00H corresponds to the data in SEG1-SEG8 as shown in the table below.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	GRID1(00H)
B7	B6	B5	B4	B3	B2	B1	B0	

2. Driving common anode LEDs:

Figure (8)

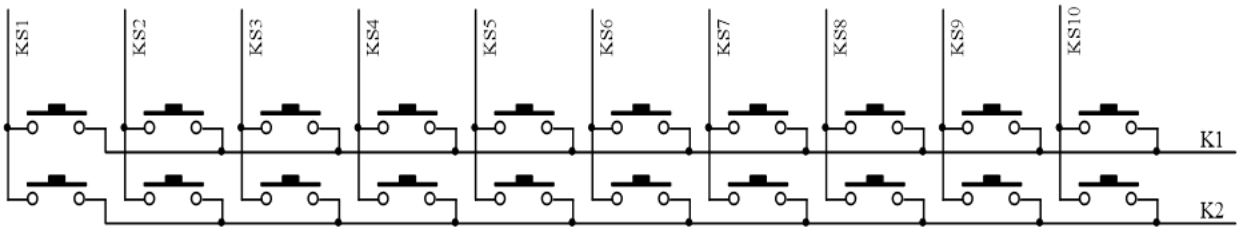
Figure 8 is a diagram for the wiring of common anode LEDs. To display 0 off the LED segment display, customers only need to write O1H into 00H (GRID1), 02H (GRID2), 04H (GRID3), 06H (GRID4), 08H (GRID5),and 0AH (GRID6), and 00H into 0CH (GRID7). SEG1-SEG8 correspond to the data table below.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	GRID1(00H)
0	0	0	0	0	0	0	1	GRID2(02H)
0	0	0	0	0	0	0	1	GRID3(04H)
0	0	0	0	0	0	0	1	GRID4(06H)
0	0	0	0	0	0	0	1	GRID5(08H)
0	0	0	0	0	0	0	1	GRID6(0AH)
0	0	0	0	0	0	0	0	GRID7(0CH)
B7	B6	B5	B4	B3	B2	B1	B0	

▲ Note: To drive common cathode LEDs or common anode LEDs, SEG pins can only be connected with LED anode, and GRID, only with LED cathode. Do not connect them in reverse direction.

VIII Keyboard scan and data register

Keyboard scan matrix is 10×2bit，as follows：



Figure（9）

The storage address of keyboard scan is shown as following chart, after send the reading key command, start reading Byte 1~ Byte 5 of key data which output from low bit. B6 and B7 are invalid bits which output is 0 at this time. When press the keys correspond with the pins of chip K and KS, corresponding bit within the byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K1	K2	K3	K1	K2	K3	X	X	
KS1			KS2			0	0	**BYTE1**
KS3			KS4			0	0	**BYTE2**
KS5			KS6			0	0	**BYTE3**
KS7			KS8			0	0	**BYTE4**
KS9			KS10			0	0	**BYTE5**

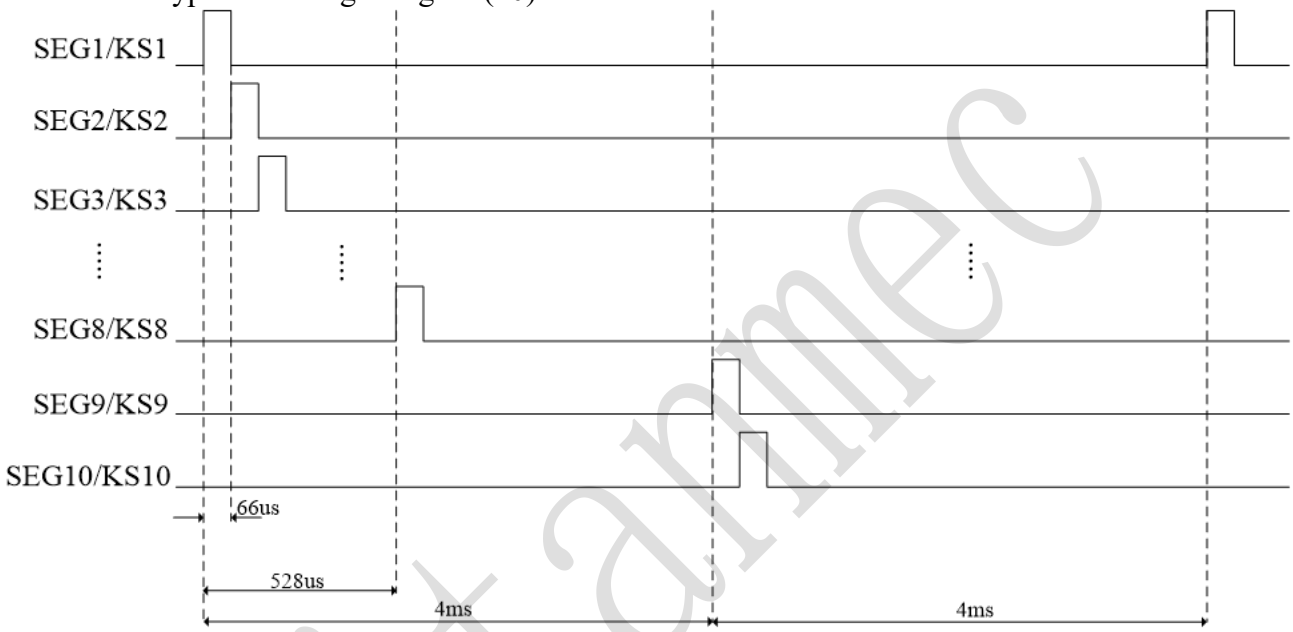
▲ **Note:** 1. TM1623 read 5 bytes maximum, more reading is not allowed.

2. Data byte can be read only from Byte 1~ Byte 5 in sequence, it can not be read across the byte. For example, when press the key correspond with the K2 and KS10, if need read data of this key, must read till the fifth bit of Byte 5.

IX、Keyboard

(1) Keyboard scan

Keyboard scanning is automatically done by TM1632 without user control. Users only need to read key codes according to time sequence. It takes two display cycle to complete one time keypad scanning, a display cycle takes about T=4ms. During this 8ms, if two different keys are pressed, the key code read in both times is the one of the key pressed first. At 7Grids11Segs mode, the SEG1/KS1～SEG10/KS10 waveform of keypad scanning as figure (10):



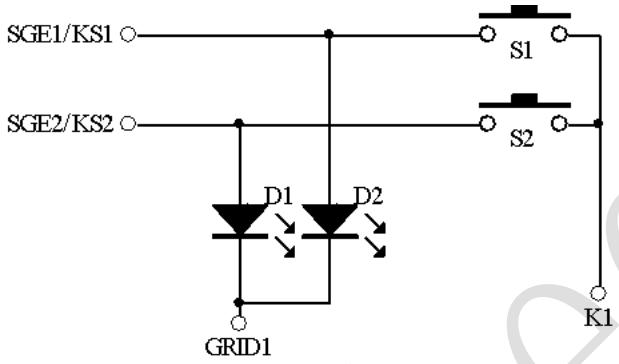
Figure（10）

As the figure (5), the principle of chip keyboard scanning as below:
Scanning start from SEG1/KS1 to SEG10/KS10, SEG1/KS1-SEG8/KS8 finish at the same cycle and SEG9/KS9-SEG10/KS10 at the next cycle. When send the reading key command, if the key scanning high level of the SEG1/KS1-SEG10/KS10 input to the K1/K2/K3 by pressing the keyboard, the chip will output high level data at the corresponding bit.

▲**Note:** Display cycle is related on the oscillation frequency of IC, the oscillation frequency is not exactly the same, please to respect the actual measurement.

(2) Combination keys

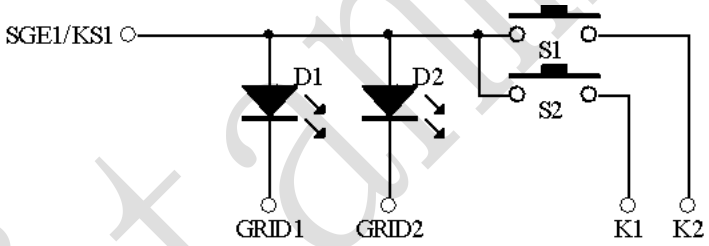
Unusual problems with combination keys: SEG1/KS1-SEG10/KS10 are for combined use for display and key scanning. Take figure (11) for example, to turn D1 on and D2 off, we have make sure SEG1 is in the status of "0"and SEG2 is in the status of "1". If S1 and S2 are pressed simultaneously, it is to the effect that SEG1 and SEG2 are short-circuited, and then D1 and D2 are turn on.



Figure（11）

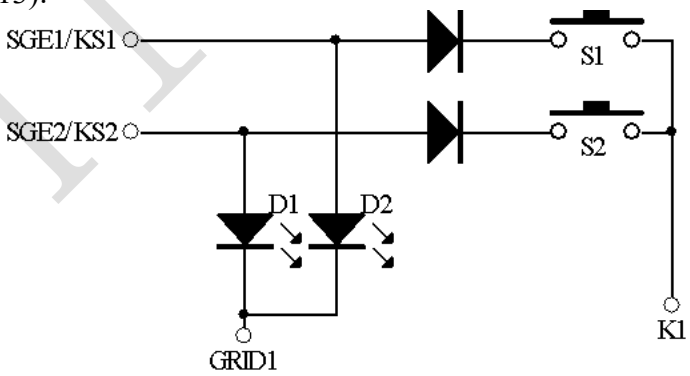
Solution:

1. In terms of hardware, it is advisable to arrange the keys to be pressed at the same time on different K line, as figure (12):



Figure（12）

2. Series diodes as figure (13):



Figure（13）

▲**Note:** It is recommend to use combination keys on the same KS but different K pin.

X. Transmission format of serial data:

A BIT is received at rising edge of the clock.

Data reception (write data)

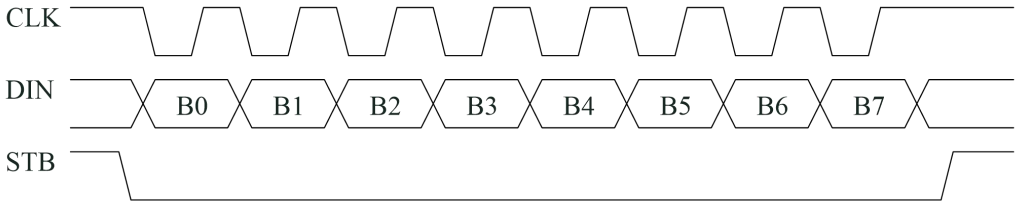
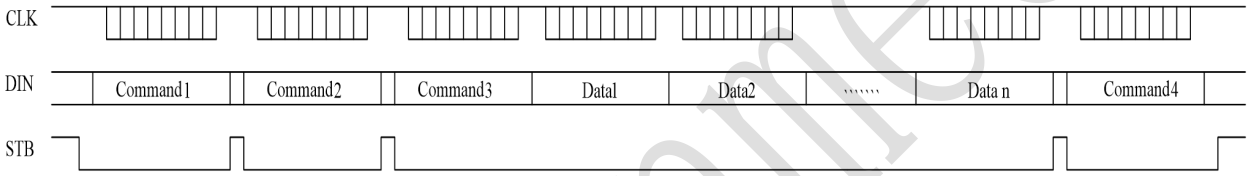


Figure (14)

XI. Transmission of serial data in application:

(1) Address increment mode

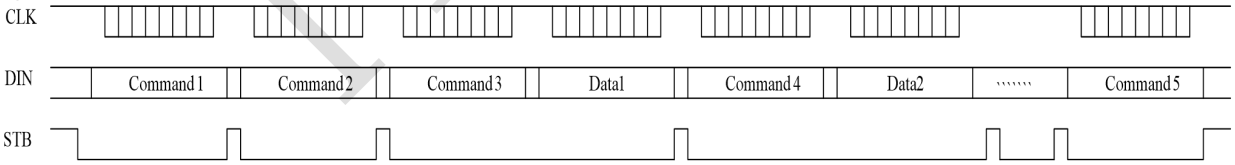
If address automatically increments by 1, the essence of address setting is to set the starting address where a data stream transmitted is stored. After the command word of the Starting Address has been sent, "STB" does not need to be set high to transmit data immediately thereafter, given 14 BYTEs at most. It is advisable to set STB high after data transmission.



Command1: Set display mode
Command2: Set data command
Command3: Set display address
Data1～ n: Transmit display data to the Command3 address and the following addresses (14 bytes at most)
Command4: Set display control command

(2) Fixed Address Mode

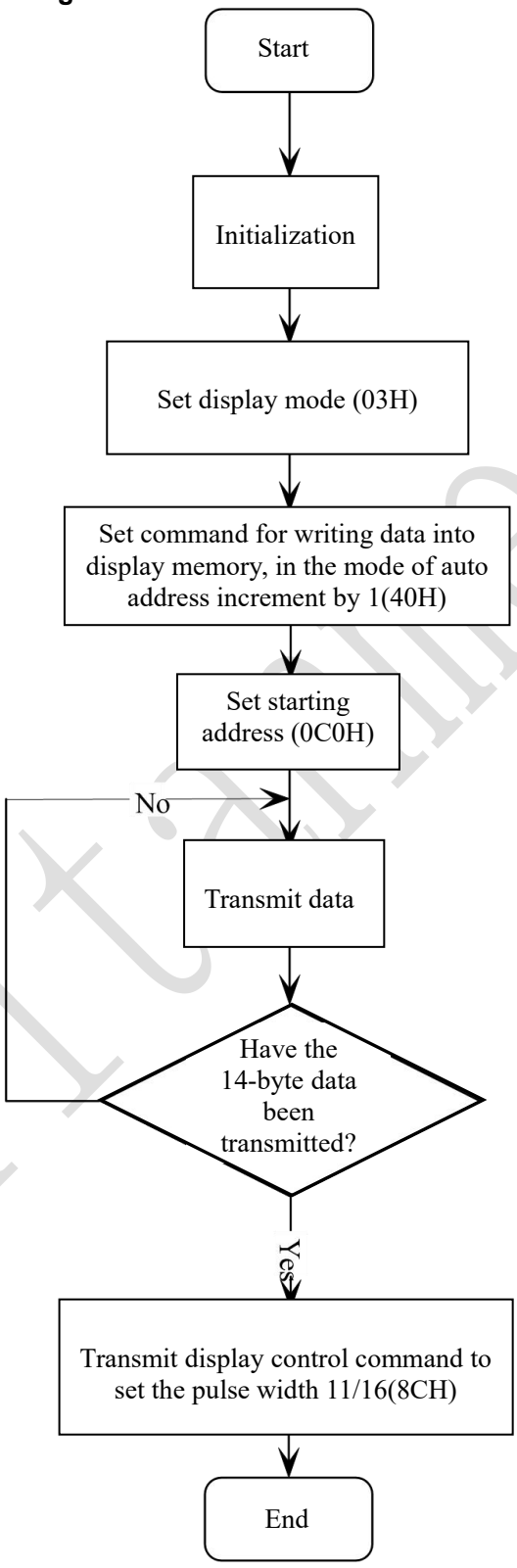
If fixed address mode is adopted, the essence of address setting is to set the address where 1 BYTE data to be transmitted is stored. After transmission of address, it is not necessary to set "STB" high to transmit 1BYTE data immediately thereafter. It is advisable to set STB high after data transmission. Then users may set the address where the second data is stored. After transmission of date up to 14 BYTES at most, "STB" is set high.



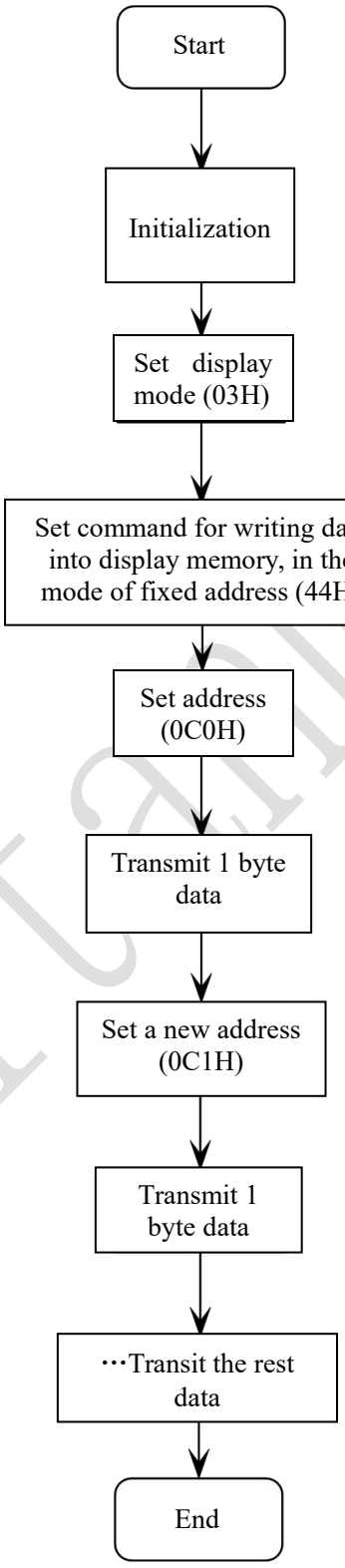
Command1: Set display mode
Command2: Set data command
Command3: Set display address1
Data1: Transmit display data 1 to Command3 address
Command4: Set display address 2
Data2: Transmit display data 2 to Command4 address
Command5: Set display control command

(4) Flowchart for program design in the modes of auto address increment by 1 and fixed address:

Flow chart for program design in the mode of auto address increment by 1:



Flowchart for program design in the mode of fixed address:



XII.. Application Circuit:

Hardware circuit diagram for TM1623 to drive a common cathode LED screen (18):

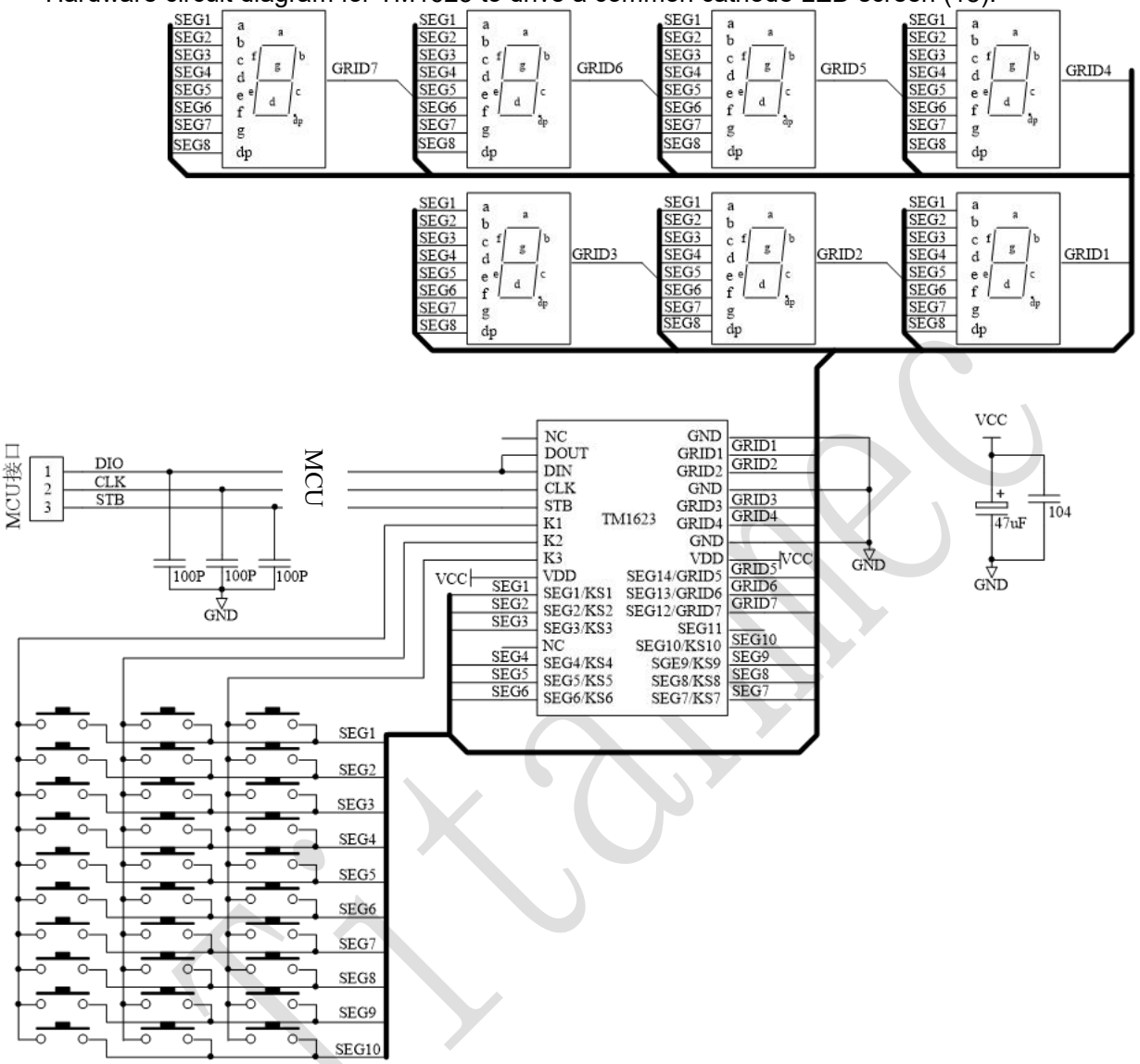


Figure (15)

Hardware circuit diagram for TM1623 to drive a common anode LED screen (19):

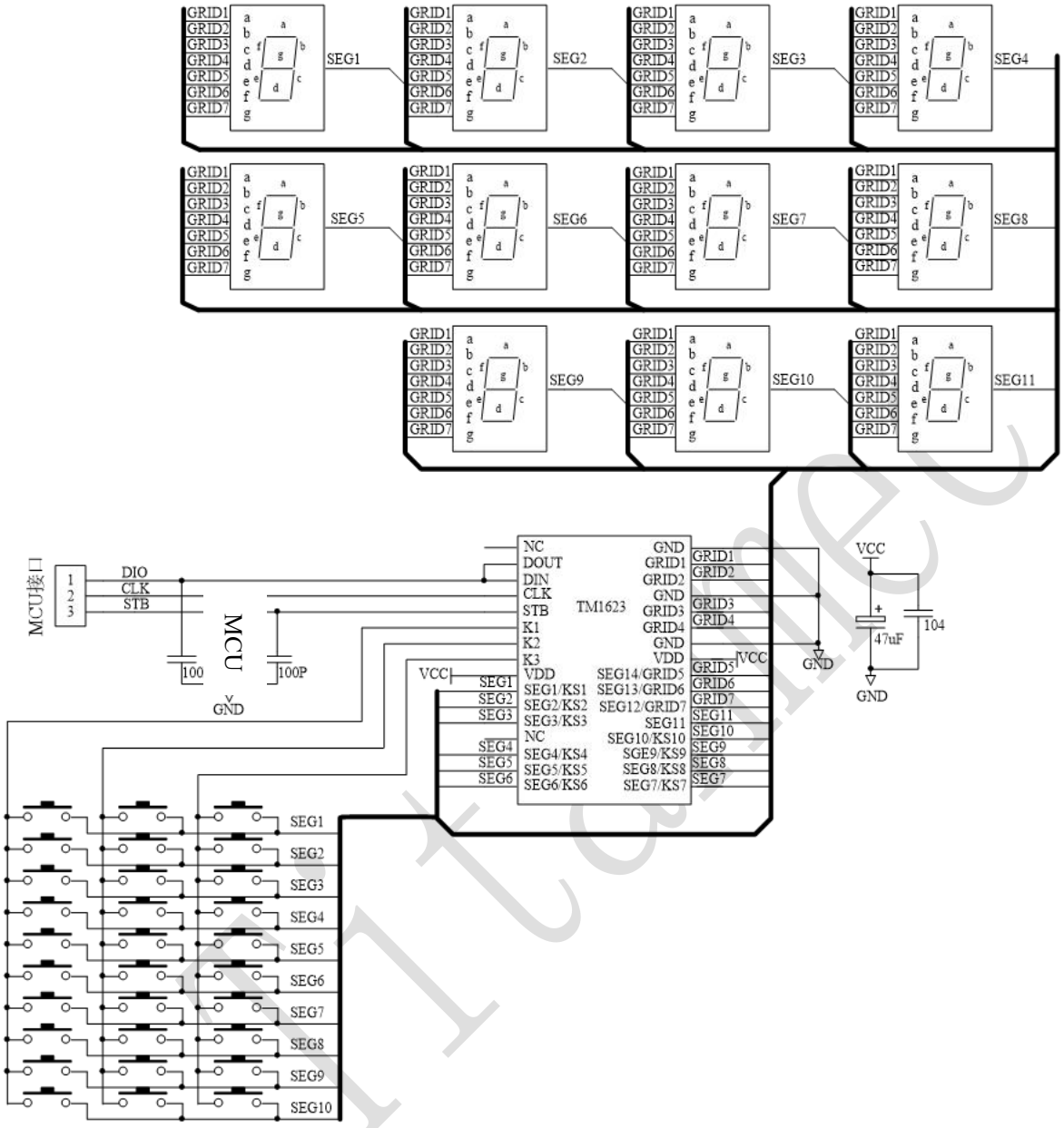


Figure (16)

▲ **Note**: 1. During PCB board wiring, the filter capacitor between VDD and GND shall be placed as close as possible to TM16234 to strengthen the filtering effect.

2. The three 100pF capacitors connected to the three communication ports, DIN, CLK, and STB will reduce interference with the communication ports.

3. Considering the turn-on voltage drop of blue digital led display is about 3V, the power supply for TM1623 should be 5V.

XIII. Electrical Parameters:

Limit parameter (Ta = 25 ℃, Vss = 0V)

Parameter	Symbol	Scope	Unit
Logic Supply Voltage	VDD	-0.5～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
Output current for LED SEG drive	IO1	-50	mA
Output current for LED Grid drive	IO2	+200	mA
Power loss	PD	400	mW
Operating temperature	Topt	-40 ～ +85	℃
Storage temperature	Tstg	-65～+150	℃
ESD	MM (Machine Mode)	200	V
	HBM (Human Body Mode)	2000	V

Normal operating range (Vss = 0V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Logic Supply Voltage	VDD	3	5	6	V	-
High-level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low-level input voltage	VIL	0	-	0.3 VDD	V	-

Electrical Characteristics （**VDD = 5V, V_{SS} = 0V**）

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
High-level output current	Ioh1	20	35	60	mA	SEG1～SEG11, Vo = VDD -3V
Low-level input voltage	I_{OL}	80	120	-	mA	GRID1～GRID7 Vo=0.3V
Tolerance of high-level output current	Itolsg	-	-	5	%	Vo = VDD – 3V, SEG1～SEG11
High-level input voltage	VIH	0.7 VDD	-		V	CLK,DIN,STB
Low-level input voltage	VIL	-	-	0.3 VDD	V	CLK,DIN,STB

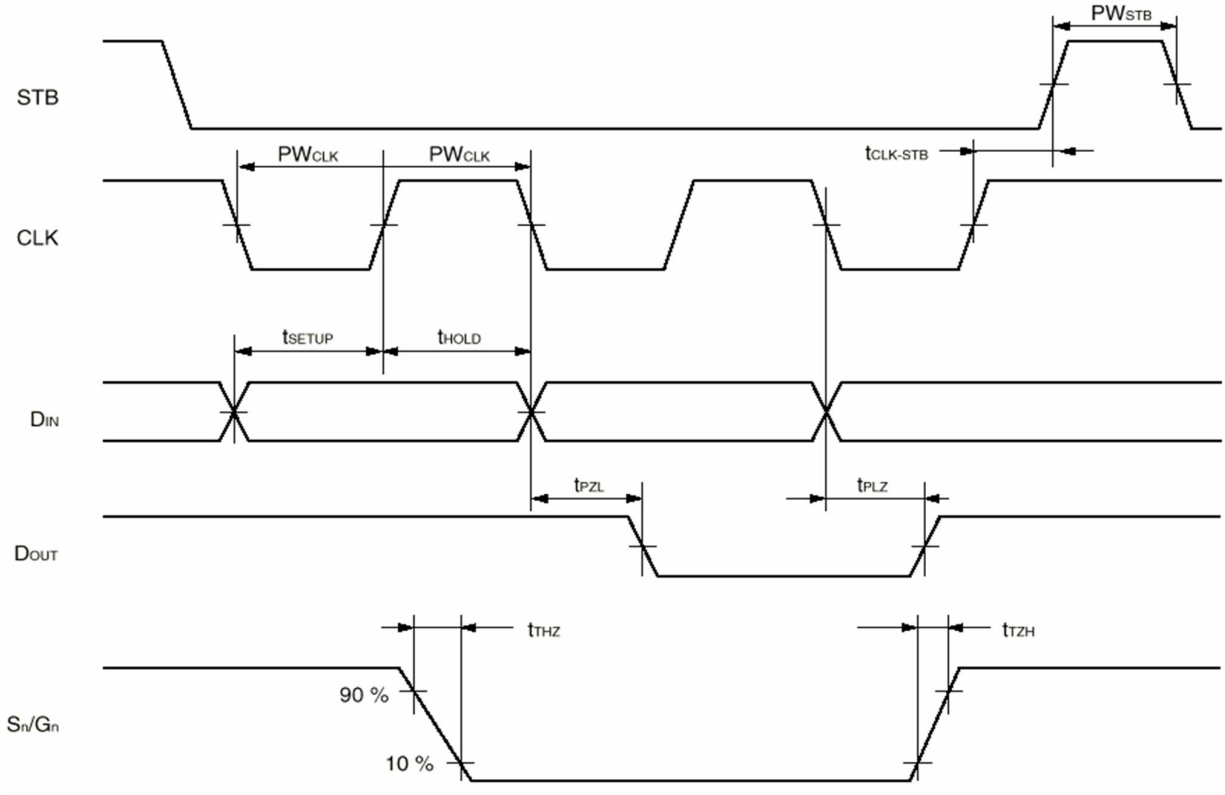
Switching Characteristics （ VDD = 5V）

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions	
Transmission delay time	t_{PLZ}	-	-	300	ns	CLK → DIN	
	t_{PZL}	-	-	100	ns	CL = 15pF, RL = 10K Ω	
Rise Time	t_{TZH1}	-	-	2	μs	CL = 300p F	SEG1～SEG11
	t_{TZH2}	-	-	0.5	μs		GRID1～GRID4 SEG12/GRID7 ～ SEG14/GRID5
Fall Time	t_{THZ}	-	-	1.5	μs	CL = 300pF,SEGn,GRIDn	
Maximum input clock frequency	Fmax	-	-	1	MHz	Duty ratio=50%	
Input capacitance	CI	-	-	15	pF	-	

Timing Characteristics （VDD = 5V）

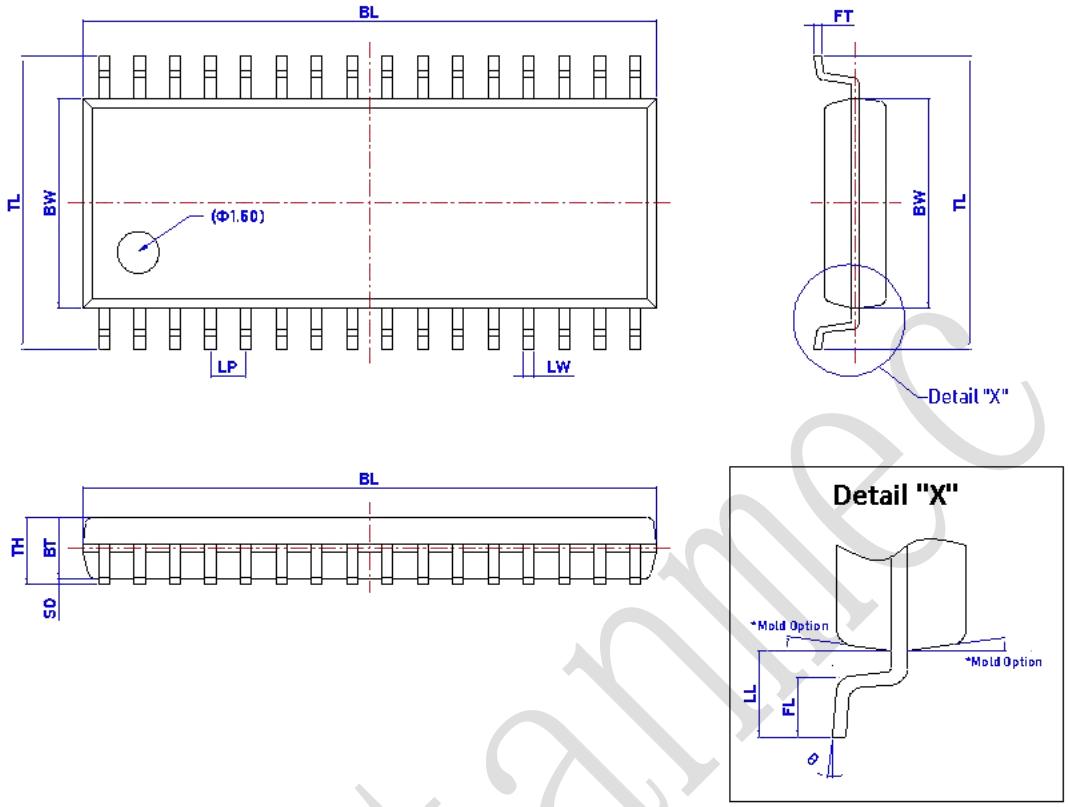
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Clock pulse width	PW_{CLK}	500	-	-	ns	-
Strobing pulse width	PW_{STB}	1	-	-	μs	-
Data setup time	t_{SETUP}	100	-	-	ns	-
Data Hold Time	t_{HOLD}	100	-	-	ns	-
CLK → STB time	$t_{CLK-STB}$	1	-	-	μs	CLK↑→STB↑

Timing Waveforms:



XIV. Schematic diagram of IC packaging

Package size for SOP32-300:



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	长度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	°
Spec	20.73 (20.63) 20.53	7.64 (7.54) 7.44	10.60 (10.40) 10.20	0.400 TYP	1.270 TYP	0.250 (0.200) 0.170	2.34 (2.24) 2.14	0.250 (0.175) 0.100	2.490 Max.	1.60 (1.50) 1.40	0.95 (0.75) 0.55	8 (4) 0

All specs and applications shown above are subject to change without prior notice.