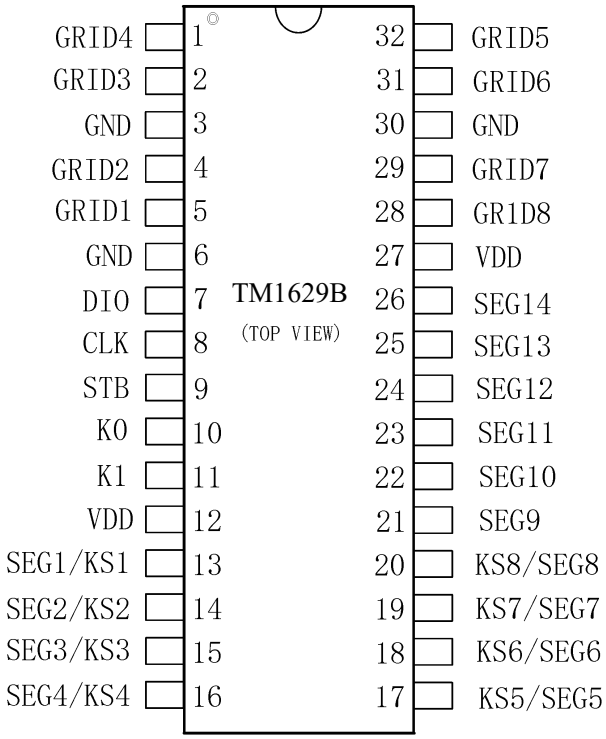
I. Overview

TM1629B is a kind of LED driver control IC with keyboard scan interface, which is integrated with MCU digital interface, data latch, LED driver, keyboard scan and other circuits. This product has reliable quality, good stability and strong anti-interference ability. It is mainly suitable for home appliances (intelligent water heater, microwave oven, washing machine, air conditioner, induction cooker), set top box, electronic scale, smart meter and other digital tube or LED display equipment.

II. Characteristic description

- **Using CMOS technology**
- **Display mode 14 segments × 8 bits**
- **Maximum support matrix key 8 × 2**
- **Brightness adjustment circuit (duty cycle 8 levels adjustable)**
- **Serial interface (CLK, STB, DIO)**
- **Oscillation mode: built in RC oscillation**
- **Built in power on reset circuit**
- **Built in data latch circuit**
- **Strong anti-interference ability**
- **Built in optimization circuit for LED reverse bias leakage leading to dark and bright problem**
- **Package form: SOP32**

III. Pin definition



IV. Pin description

Symbol	Pin name	Pin No.	Explain
DIO	Data output input	7	Input serial data at the rising edge of the clock, starting from the low bit. The serial data is output on the falling edge of the clock, starting from the low bit. The output is n-tube open drain output, external need to connect 1-10k Ω Pull up resistor to VCC
CLK	Clock input	8	The serial data is read on the rising edge and output on the falling edge
STB	Selected films	9	Initialize the serial interface on the falling edge, and then wait for the command to be received. STB is the first byte after low as an instruction. When the instruction is processed, other current processing is terminated. When STB is high, CLK is ignored
K0～K1	Key scan data input	10～11	The data input to the pin is locked after the end of the display cycle, with a built-in 7.3k Ω Pull down resistance
SEG1/KS1～ SEG8/KS8	Output (segment)	13～20	Segment output (also used as key scan), p-tube open drain output, built-in 3.6k Ω Pull down resistance
SEG9～SEG14	Output (segment)	21～26	Section output, p-tube open drain output, built-in 3.6k Ω Pull down resistance
GRID1～GRID2 GRID3～GRID4 GRID5～GRID6 GRID7～GRID8	Output (bit)	5～4 2～1 32～31 29～28	Bit output, n-tube open drain output, built-in 2.8k Ω Pull up resistor
VDD	Logic power supply	27,12	Connected to power supply
GND	Logic place	3,6,30	Grounding system

▲Note: 1, DIO port output data for n tube open drain output, in the key reading time need external 1k-10k pull-up resistance. The company recommends 10K pull-up resistor. Dio controls the action of n-tube at the falling edge of the clock. At this time, the reading is unstable, and the reading is stable at the rising edge.

V. Instructions:

The command is used to set the display mode and the status of the LED driver.

The first byte entered by DIN after the falling edge of STB is used as the instruction. After decoding, the highest B7 and B6 bits are selected to distinguish different instructions.

B7	B6	Instructions
0	1	Data command settings
1	0	Display control command settings
1	1	Address command settings

If STB is set to high level at the time of instruction or data transmission, serial communication is initialized, and the instruction or data being transmitted is invalid (the instruction or data transmitted previously remains valid).

（1） Data command settings:

This instruction is used to set the data write and read, B1 and B0 bits are not allowed to set 01 or 11.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Explain
0	1	Irrelevant items, fill in 0				0	0	Data read / write mode setting Address increase mode setting	Write data to display register
0	1					1	0		Read key scan data
0	1				0			Mode setting Data read / write mode setting	Automatic address increase
0	1				1				Fixed address
0	1			0				Address increase mode setting	Normal mode

（2） Display control command settings:

This command is used to set the switch of display and adjust the brightness of display. There are 8 levels of brightness to choose from.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Explain
1	0	Irrelevant items, fill in 0			0	0	0	Extinction quantity setting	Set the pulse width to 1 / 16
1	0				0	0	1		Set the pulse width to 2 / 16
1	0				0	1	0		Set the pulse width to 4 / 16
1	0				0	1	1		Set the pulse width to

								10 / 16
1	0			1	0	0		Set the pulse width to 11 / 16
1	0			1	0	1		Set the pulse width to 12 / 16
1	0			1	1	0		Set the pulse width to 13 / 16
1	0			1	1	1		Set the pulse width to 14 / 16
1	0		0				Display switch settings	Display off
1	0		1					Display on

（3） Address command settings:

This instruction is used to set the address of the display register. The maximum effective address is 16 bits (C0H-CFH). If the address is set to D0H or higher, the data is ignored until the effective address is set. When power on, the address is set to C0H by default.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	Irrelevant items, fill in 0		0	0	0	0	C0H
1	1			0	0	0	1	C1H
1	1			0	0	1	0	C2H
1	1			0	0	1	1	C3H
1	1			0	1	0	0	C4H
1	1			0	1	0	1	C5H
1	1			0	1	1	0	C6H
1	1			0	1	1	1	C7H
1	1			1	0	0	0	C8H
1	1			1	0	0	1	C9H
1	1			1	0	1	0	CAH
1	1			1	0	1	1	CBH
1	1			1	1	0	0	CCH
1	1			1	1	0	1	CDH
1	1			1	1	1	0	CEH
1	1			1	1	1	1	CFH

VI. Display register address:

The register stores the data transmitted from the external device to TM1629B through the serial interface. The most effective address is fromC0H-CFH, with a total of 16 byte units, corresponding to the chip SEG and GRID pins respectively. The specific allocation is shown in figure (2)

When writing LED display data, operate from low bit to high bit of display address and from low bit to high bit of data byte.

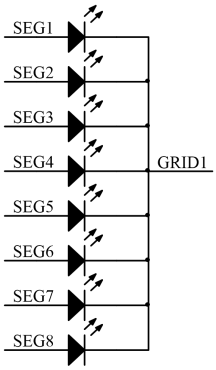
SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	X	X	
xxHL（Lower four bits）				xxHU(Higher four bits)				xxHL(Lower four bits)				xxHU（Higher four bits）				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
C0HL				C0HU				C1HL				C1HU				**GRID1**
C2HL				C2HU				C3HL				C3HU				**GRID2**
C4HL				C4HU				C5HL				C5HU				**GRID3**
C6HL				C6HU				C7HL				C7HU				**GRID4**
C8HL				C8HU				C9HL				C9HU				**GRID5**
CAHL				CAHU				CBHL				CBHU				**GRID6**
CCHL				CCHU				CDHL				CDHU				**GRID7**
CEHL				CEHU				CFHL				CFHU				**GRID8**

Fig（2）

▲Note: the value of chip display register stored in the power on moment may be random and uncertain. At this time, the customer sends the open screen command directly,
It is possible to display garbled code. Therefore, our company suggests the customer to perform a power on reset operation on the display register, that is, after power on, write all the data 0x00 to the 16 bit video memory address (00H-0FH).

VII. Display:

1. Drive common cathode nixie tube



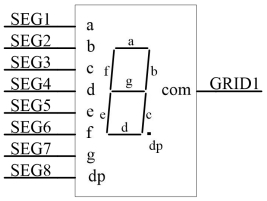


Fig.（7）

Figure 7 shows the connection diagram of the common cathode digital tube. If the nixie tube displays "0", you only need to write the data of 0x3f to the address of C0H (GRID1) from the low position. At this time, the data of C0H corresponding to each SEG1-SEG8 is shown in the table below.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	GRID1(C0H)
B7	B6	B5	B4	B3	B2	B1	B0	

2. Digital tube driving common anode

Fig.（8）

Figure 8 shows the connection diagram of common anode digital tube. If the digital tube displays "0", it is necessary to write data 01H to address units C0H(GRID1),C2H(GRID2),C4H(GRID3),C6H(GRID4),C8H(GRID5),CAH(GRID6) respectively, and write data 00h to other address units CCH (grid7) and CEH (grid8). The corresponding data of each SEG1-SEG8 is shown in the table below.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	GRID1(C0H)
0	0	0	0	0	0	0	1	GRID2(C2H)
0	0	0	0	0	0	0	1	GRID3(C4H)
0	0	0	0	0	0	0	1	GRID4(C6H)
0	0	0	0	0	0	0	1	GRID5(C8H)
0	0	0	0	0	0	0	1	GRID6(CAH)
0	0	0	0	0	0	0	0	GRID7(CCH)
0	0	0	0	0	0	0	0	GRID8(CEH)
B7	B6	B5	B4	B3	B2	B1	B0	

▲Note: whether driving common cathode digital tube or driving common anode digital tube, SEG pin can only be connected to the anode of LED, grid can only be connected to the cathode of LED, not reversed.

VIII. Key scan and key scan data register:

The maximum key scan matrix of the chip is 8 × 2bit, as shown in figure (3)

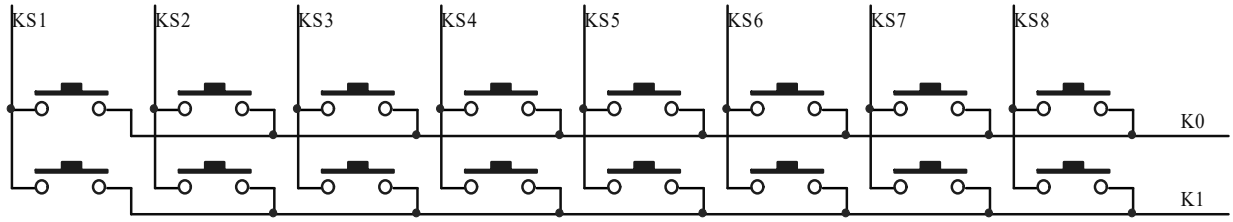


Fig.（3）

The key scan data storage address is shown in figure (4). After the command of key reading is issued first, byte 1-byte 4 of key data is read. The read data is output from the low bit. When the key corresponding to the K and KS pins of the chip is pressed, the bit bit in the corresponding byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7
X	X	K1	K0	X	X	K1	K0

KS1	KS2	BYTE1
KS3	KS4	BYTE2
KS5	KS6	BYTE3
KS7	KS8	BYTE4

Fig.（4）

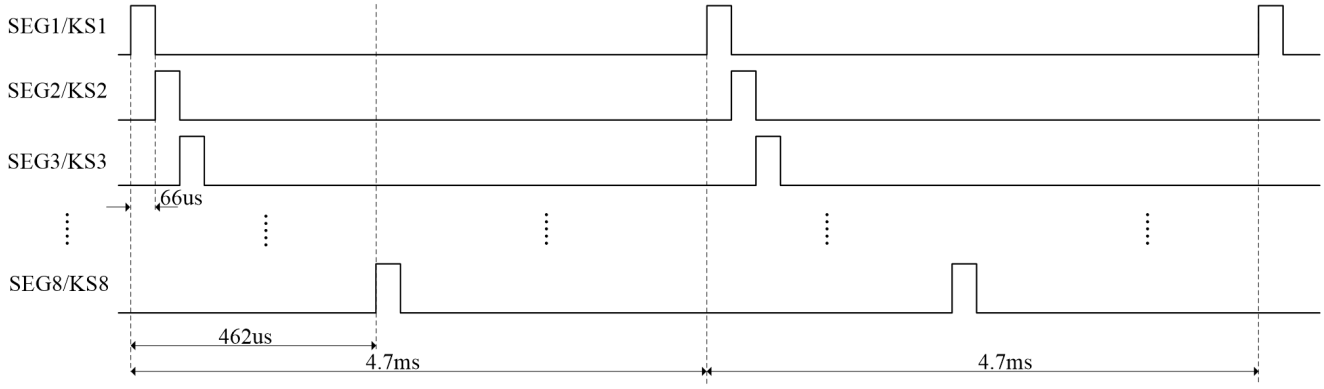
Note:

1. TM1629b can read 4 bytes at most, and it is not allowed to read more.
2. Read data bytes can only be read from byte1-byte4 in sequence, not across bytes. For example, when K2 and KS8 on the hardware are pressed, if you want to read the key data, you must read the sixth bit of the fourth byte before you can read the data.

IX. Key:

(1) Key scanning: the key scanning is automatically completed by tm1629b, which is not controlled by the user. The user only needs to read the key value according to the sequence. One display cycle is needed to complete a key scan, and one display cycle needs t = 4.7ms. Two different keys are pressed successively within 4.7ms, and the key value read twice is the key value of the first key pressed.

After the TM 1629b is powered on, the waveform of SEG1/KS1-SEG8/KS8 is shown in figure (10)



Fig（10）

▲Note: one cycle time is related to the oscillation frequency of IC, and the oscillation frequency of each IC is not completely consistent. The above data are for reference only, subject to the actual measurement.

（**2**）**Key reuse**: the problem of composite key is abnormal: SEG1/KS1-SEG8/KS8 is display and key scan reuse. Taking figure (12) as an example, it shows that D1 needs to be on and D2 off, SEG1 needs to be "0" and seg2 is "1". If S1 and S2 are pressed at the same time, it is equivalent to SEG1 and SEG2 being short circuited. At this time, D1 and D2 are on.

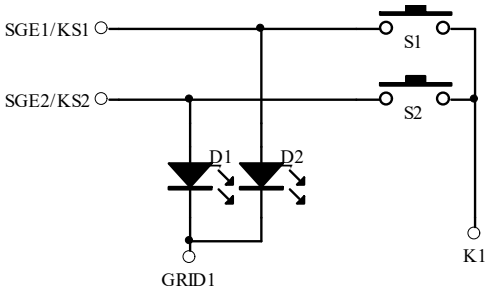
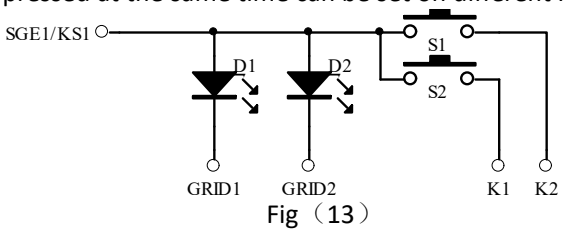


Fig.（12）

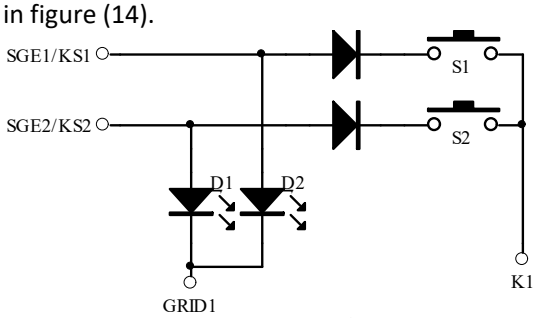
Solution:

1. On the hardware, the keys to be pressed at the same time can be set on different K lines, as shown in figure (13),



Fig（13）

2. The diode in series is shown in figure (14).



Fig（14）

▲Note: it is recommended to use the same KS different K key as the composite key.

X. Serial data transmission format:

Reading and receiving a bit operate on the rising edge of the clock

Data receiving (data writing)

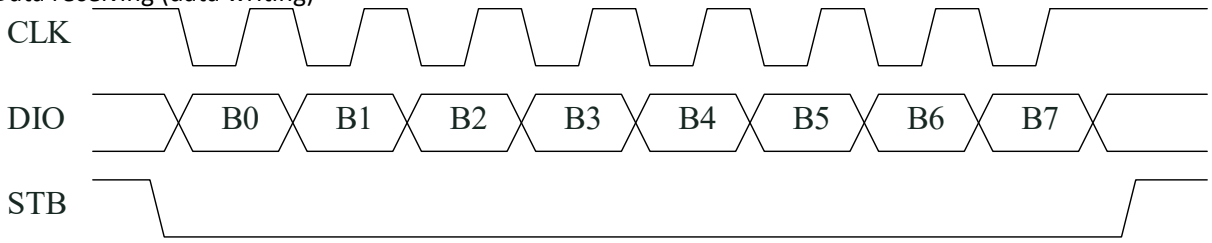


Fig.（5）

Data reading (data reading)

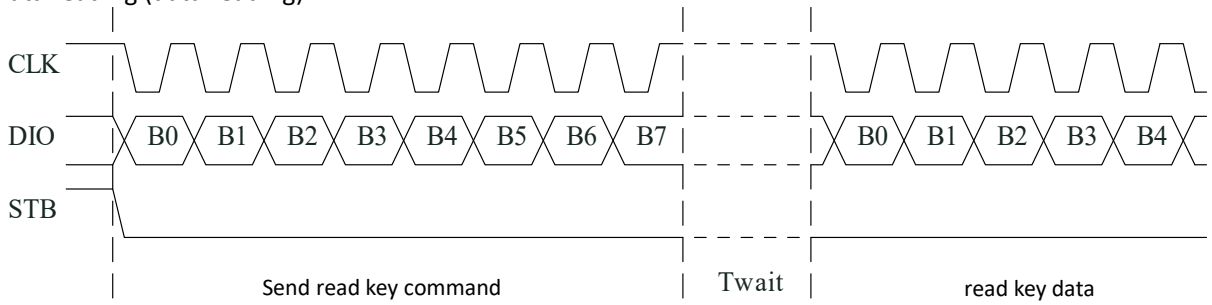


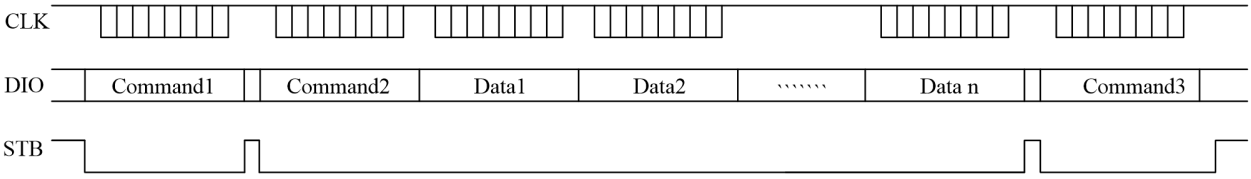
Fig.（6）

▲Note: 1. When reading data, there is a waiting time between the instruction setting from the eighth rising edge of the serial clock CLK and the data reading from the falling edge of CLK (minimum 2μS). See the time sequence characteristic table for specific parameters.

XI. Serial data transmission in application:

(1) Address increase mode

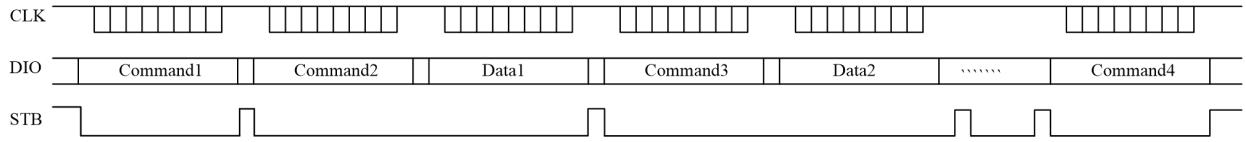
Using the mode of address auto plus 1, setting the address is actually setting the starting address of the data stream. After the start address command word is sent, "STB" does not need to be set high to transfer data immediately. At most, it is 16byte. After the data is transferred, "STB" is set high.



Command1: set data command
Command2: set display address
Data1-n: transfer display data to command2 address and later address (up to 16bytes)
Command3: display control command

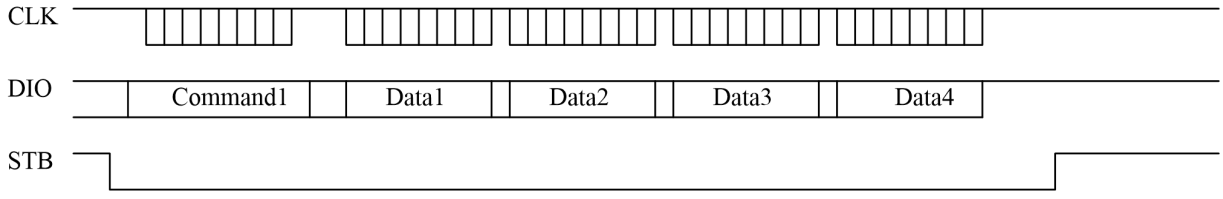
（2） Fixed address mode

Using the fixed address mode, setting the address is actually setting the address where the 1byte data to be transmitted is stored. After the address is sent, "STB" does not need to be set high, but 1byte data is transferred immediately, and "STB" is set high after data transmission. Then reset the address where the second data needs to be stored. After the 16byte data transmission is completed, set "STB" high.



Command1: set data command
Command2: set display address 1
Data1: transfer display data 1 to the address of command2
Command3: set display address 2
Data2: transfer display data 2 to the address of command3
Command4: display control command

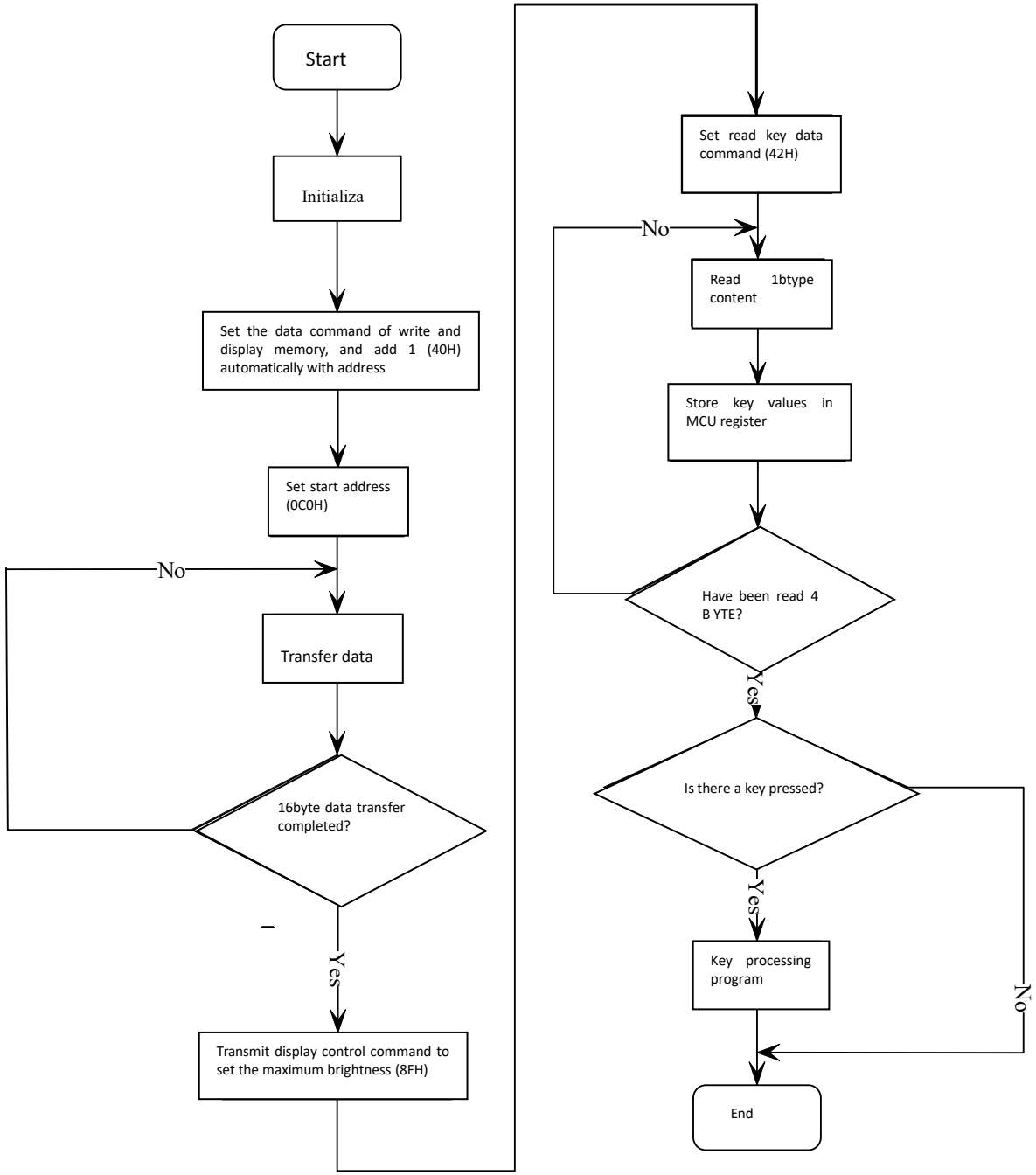
（3）Read key timing



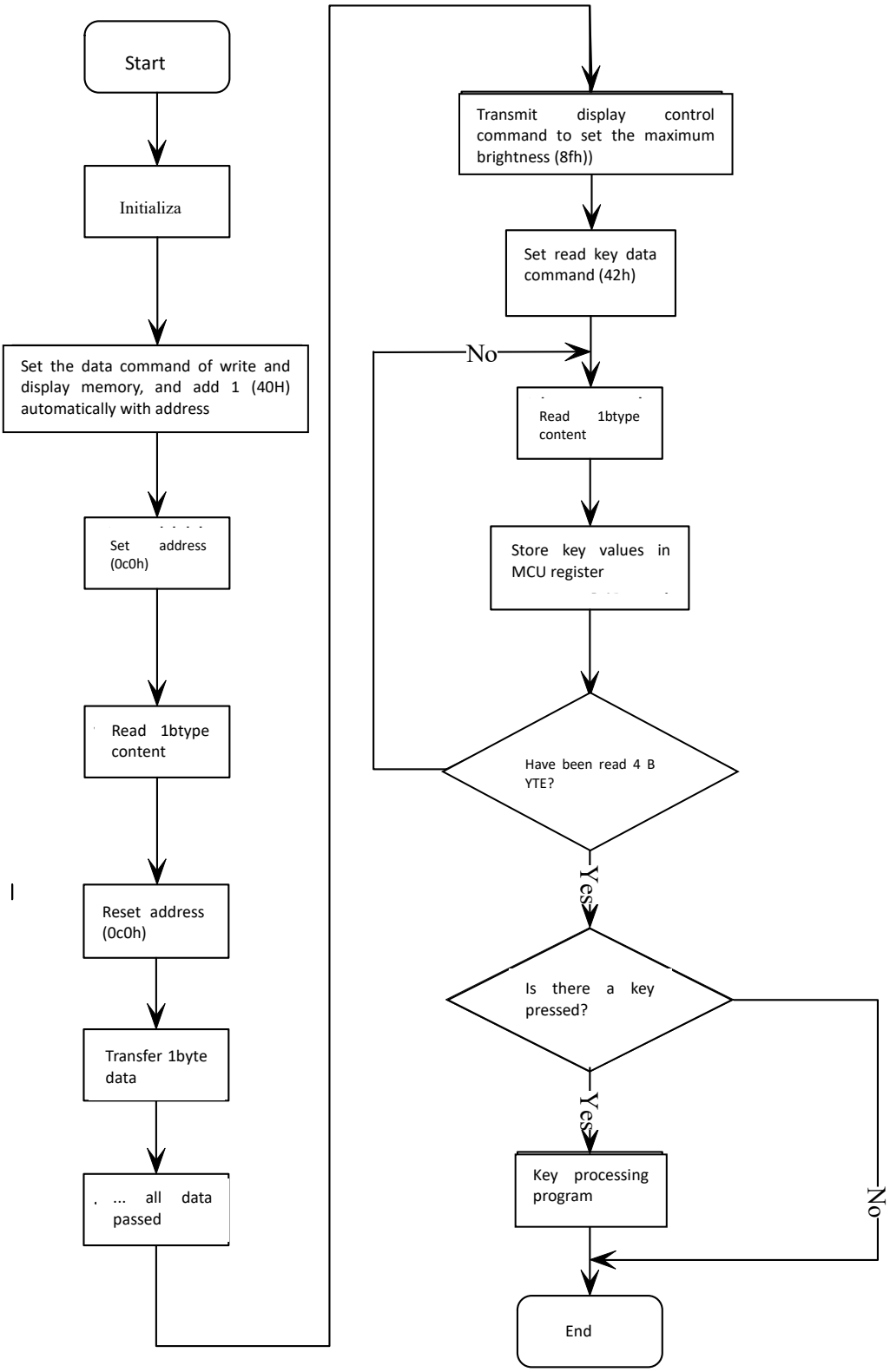
Command1: set read key command
Data1-4: read key data

（4）The flow chart of program design with address auto plus one and fixed address mode is as follows

The flow chart of program design with automatic address plus one is as follows

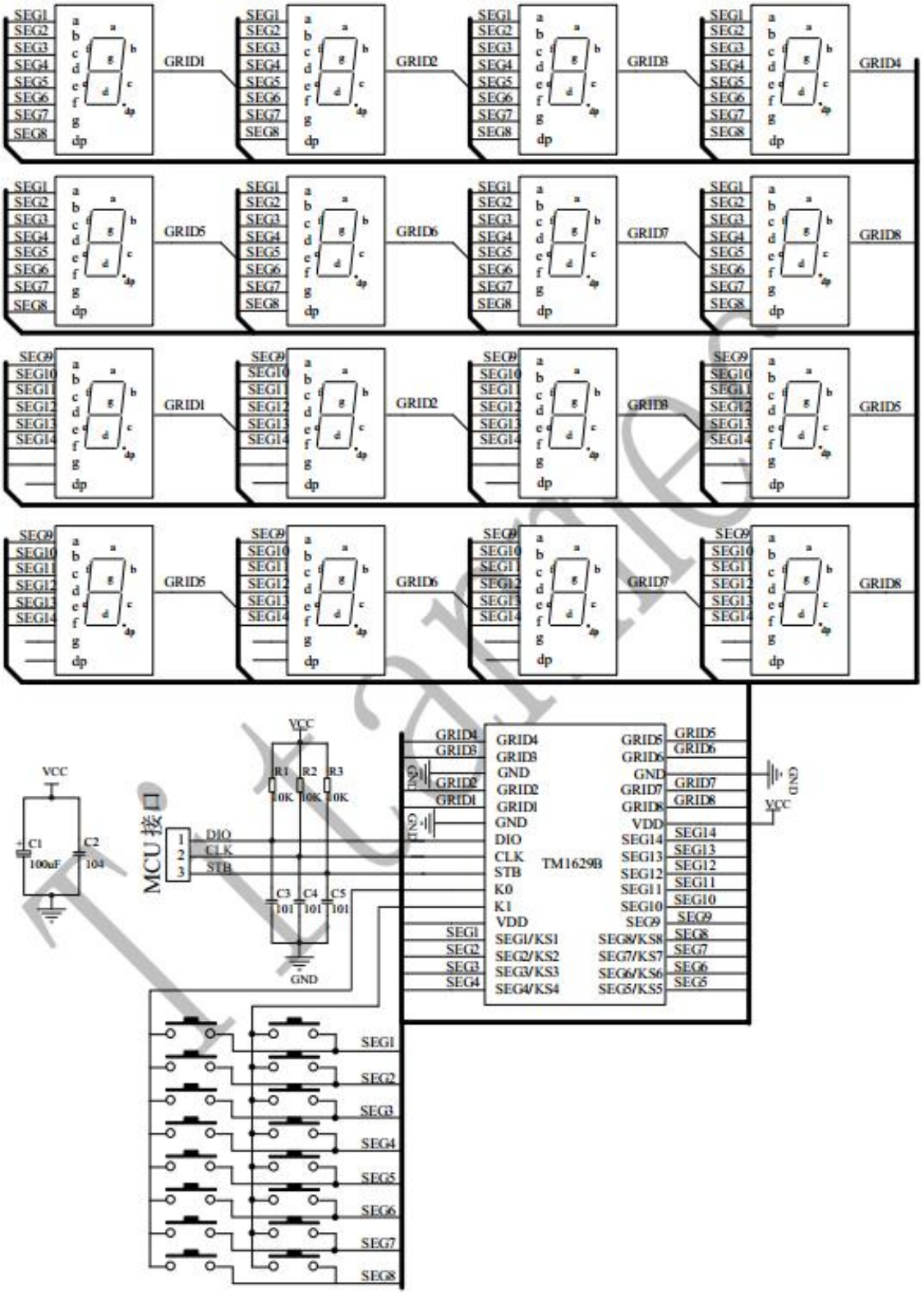


Flow chart of program design with fixed address:



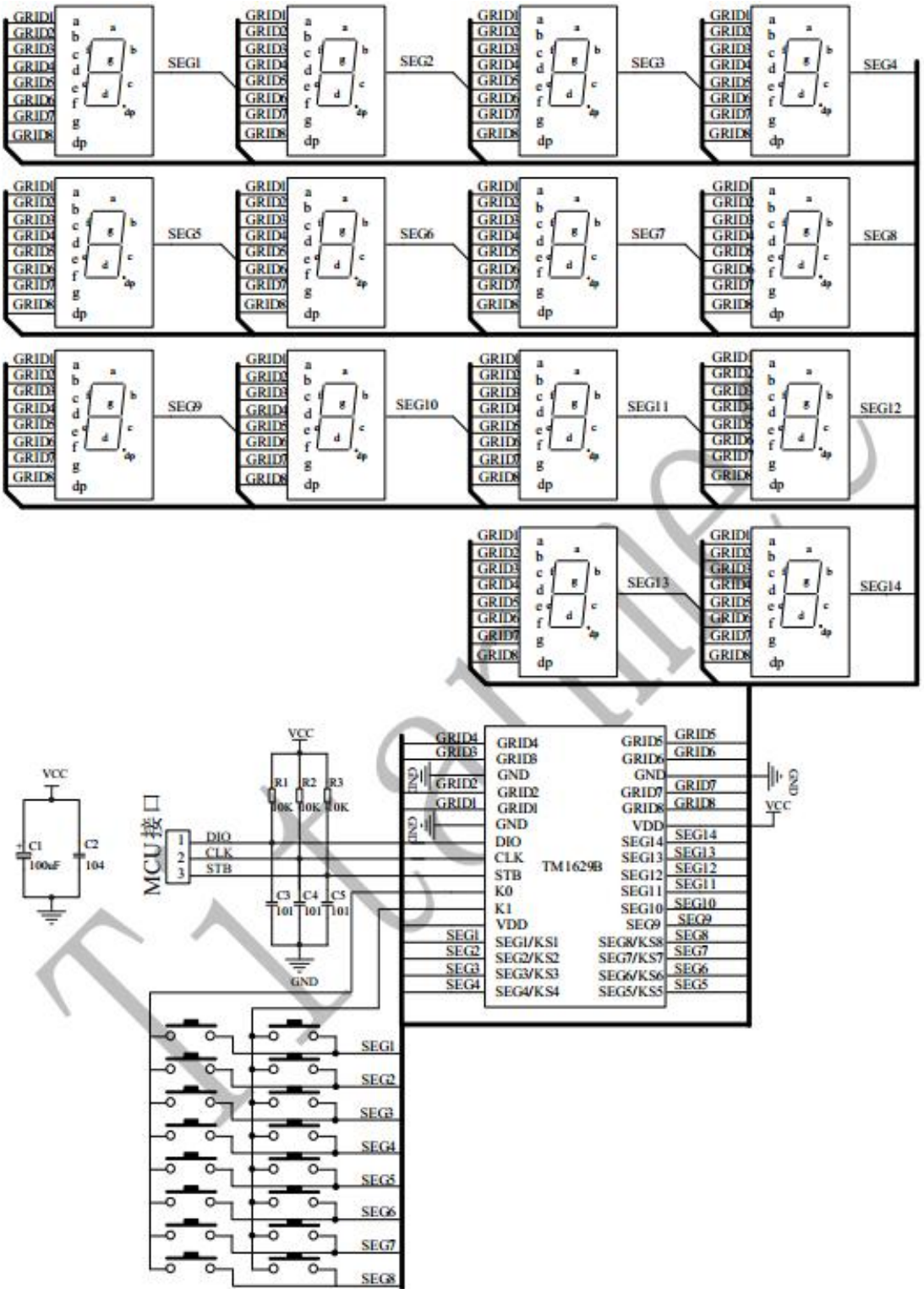
XII. Application circuit:

Hardware circuit diagram of tm1629b driving common cathode digital screen



Fig（18）

TM1629B drive common positive digital screen wiring circuit diagram (19)



Fig（19）

▲Note:

1. The filter capacitor between VDD and GND should be placed close to TM1629B chip in PCB wiring to enhance the filtering effect.
2. Three 101 (100pF) capacitors connected to DIO, SCLK and STB communication ports can reduce the interference to communication ports.
3. Because the conduction voltage of blue LED is about 3V, the power supply of TM1629B should be 5V.

XIII. Electrical parameters:

Limit parameter (TA = 25 ℃, VSS = 0V)

Parameter	Symbol	Scope	Unit
Logic supply voltage	VDD	-0.5 ～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
Led SEG drive output current	IO1	-50	mA
Led grid drive output current	IO2	+200	mA
Power loss	PD	400	mW
Working temperature	Topt	-40 ～ +85	℃
Storage temperature	Tstg	-65 ～+150	℃

Normal operating range（Vss = 0V）

Parameter	Symbol	Min	Typical	Max	Unit	Test conditions
Logic supply voltage	VDD	3	5	6	V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

Electrical characteristics（VDD = 5 V, Vss = 0V）

Parameter	Symbol	Min	Typical	Max	Unit	Test conditions
High level output current	Ioh	20	35	50	mA	SEG1～SEG14, Vo = VDD – 3V
Low level input current	I_{OL1}	80	140	-	mA	GRID1～GRID8 Vo=0.3V
High level output current tolerance High level input voltage	Itolsg	-	-	5	%	Vo = VDD – 3V, SEG1～SEG14
Low level input voltage	VIH	0.7 VDD	-	-	V	CLK,DIO,STB
High level output current	VIL	-	-	0.3 VDD	V	CLK,DIO,STB

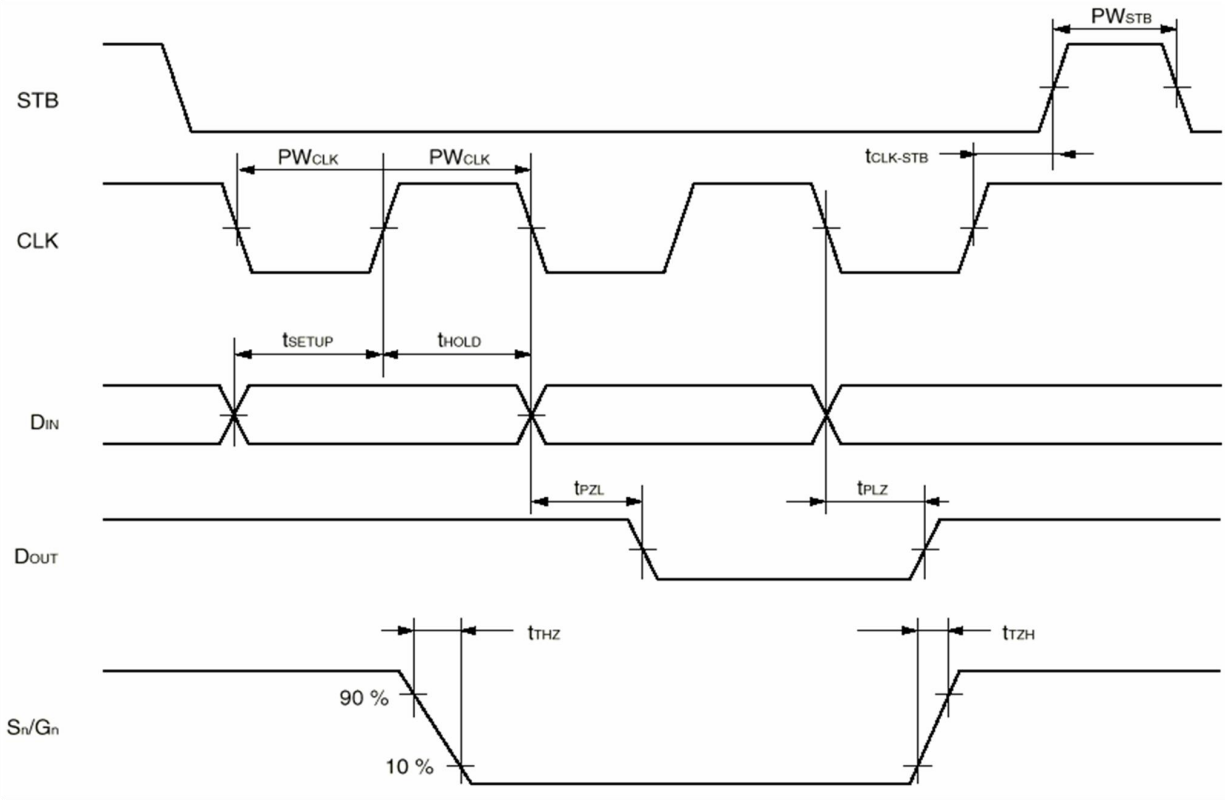
Switching characteristics（VDD = 5V）

Parameter	Symbol	Min	Typical	Max	Unit	Test conditions	
Transmission delay time	t_{PLZ}	-	-	300	ns	CLK → DIO	
	t_{PZL}	-	-	100	ns	CL = 15pF, RL = 10KΩ	
Rise time	$t_{TZH\ 1}$	-	-	2	μs	CL = 300p F	SEG1～SEG14
Descent time	t_{THZ}	-	-	1.5	μs	CL = 300pF,SEGn,GRIDn	
Maximum input clock frequency	Fmax	-	-	1	MHz	Duty cycle 50%	
Input capacitance	CI	-	-	15	pF	-	

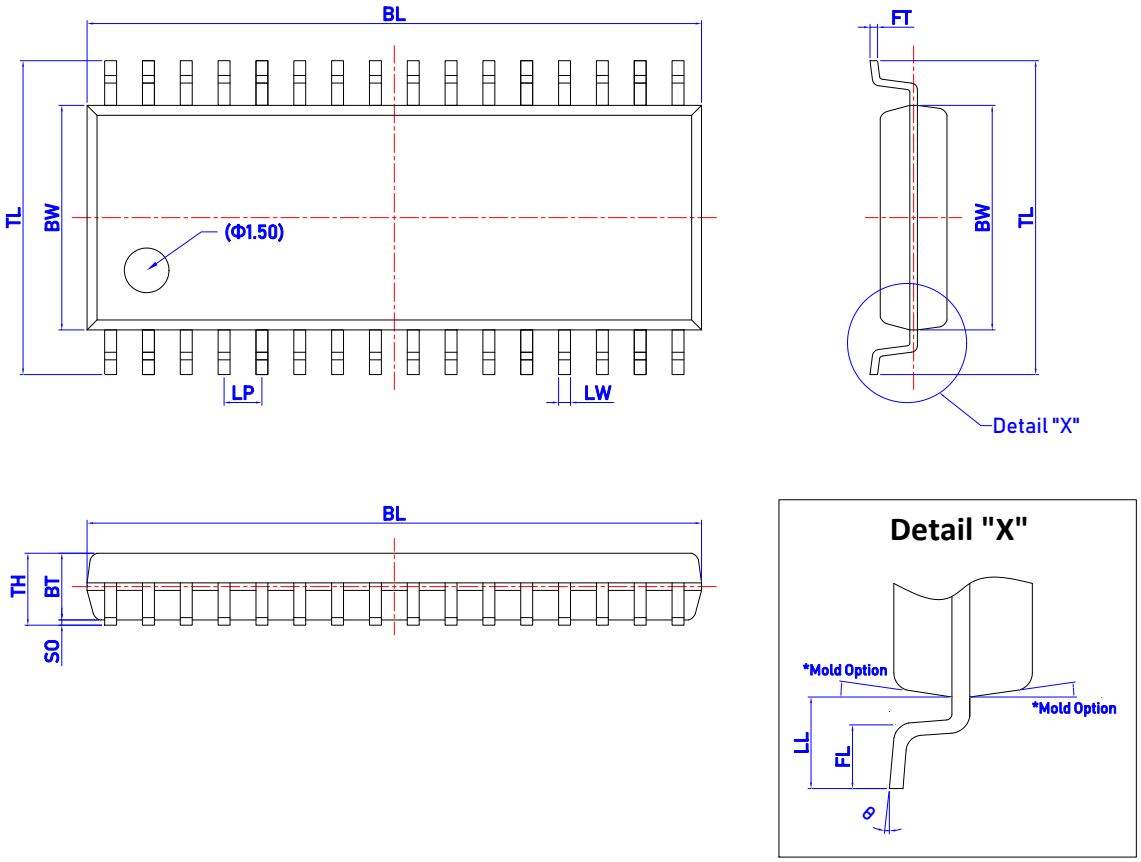
Temporal characteristic（VDD = 5V）

Parameter	Symbol	Min	Typical	Max	Unit	Test conditions
Clock pulse width	PW_{CLK}	500	-	-	ns	-
Gate pulse width	PW_{STB}	1	-	-	μs	-
Data establishment time	t_{SETUP}	100	-	-	ns	-
Data retention time	t_{HOLD}	100	-	-	ns	-
CLK → STB time	$t_{CLK-STB}$	1	-	-	μs	CLK↑→STB↑

Sequence waveform：



XIV. Package size(SOP32-300)



Di symbol ons

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	20.73 (20.63) 20.53	7.64 (7.54) 7.44	10.60 (10.40) 10.20	0.400 TYP	1.270 TYP	0.250 (0.200) 0.170	2.34 (2.24) 2.14	0.250 (0.175) 0.100	2.490 Max.	1.60 (1.50) 1.40	0.95 (0.75) 0.55	8 (4) 0

All specs and applications shown above subject to change without prior notice.