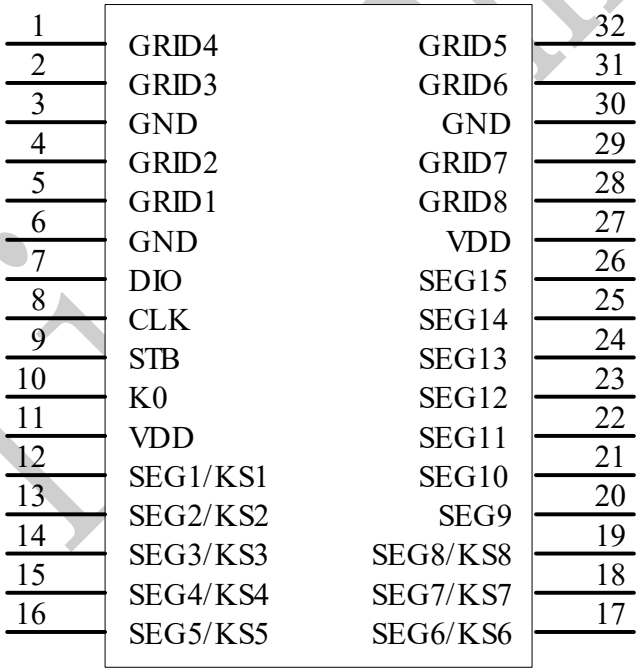
1. Description

TM1629C is LED driver control circuit with keyboard scan interface, MCU digit interface, data latch, LED high-voltage driver and keyboard scan circuit integrated into a single chip. It main apply for high segment display board driver of weighting scale, air condition, home theatre etc.

2. Feature

Use power CMOS technology
Display mode 15seg*8com
Key scan (8*1bit)
Grad adjust circuit (duty ratio 8level adjustable)
Serial interface (CLK, STB, DIO)
Oscillation type: RC oscillation (450 KHz + 5%)
Build-in power-on reset circuit
SOP32 package

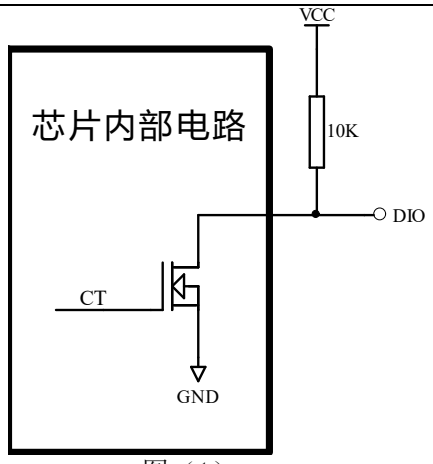
3. Pin definition



4. pin instruction

Symbol	Pin name	instruction
DIO	Data input/output	Input/out serial data at the rising edge of CLK, from low level.
STB	Chip selection	Initialize serial interface at the rising/ falling edge, then awaiting receive instruction. T he first byte as instruction after STB is low. Another deal would be final when handling the instruction. CLK would be ignore when STB is high.
CLK	Clock input	Input/output serial data when rising edge of CL
KO	Key scan data input	The data input into the pin would be latched after display period over.
SEG1/KS1~SEG8/KS8	output （segment）	Segment output (also use for key scan), P-channel open drain output, built-in 3.6k Ω Pull down resistance
SEG9~SEG15	output （segment）	Segment output, P-channel open- drain output , built-in 3.6k Ω Pull down resistance
GRID1～GRID8	output（bit）	Bit output, N-channel open- drain Output, built-in 2.8k Ω Pull up resistor
VDD	Logic power	Connect to positive pole of power
GND	Logic ground	Connect ground system

Note: DIO port output data is N-channel open-drain output, please connect 1K-10K rising resistance when read keyboard. We recommend 10K resistance. DIO control N-channel at falling edge of CLK, in that time the value is unstable. Please refer to chart6. it will stable at the rising edge of CLK.



图（1）

5. display register address and display mode:

The register stock send data to TM1629C via serial port from outer device. address from 00H-0FH total 16byte unit, separate correspond with LED light connect SGE and GRID pin of chips. As below chart:

LED display data, follow display address from low to high, and display data byte from low to high.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	X	
xxHL（low 4bi）				xxHU((high 4 bi)				xxHL(low 4bi)				xxHU（(high 4 bi）				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				GRID1
02HL				02HU				03HL				03HU				GRID2
04HL				04HU				05HL				05HU				GRID3
06HL				06HU				07HL				07HU				GRID4
08HL				08HU				09HL				09HU				GRID5
0AHL				0AHU				0BHL				0BHU				GRID6
0CHL				0CHU				0DHL				0DHU				GRID7
0EHL				0EHU				0FHL				0FHU				GRID8

Chart2

When LED display data, follow from low address to high address, low byte to high byte; if don’t use SEG output port, please input 0 to responding address.

6. Key scan and key scan data register:

Key scan matrix is 8*1bit, as chart3,

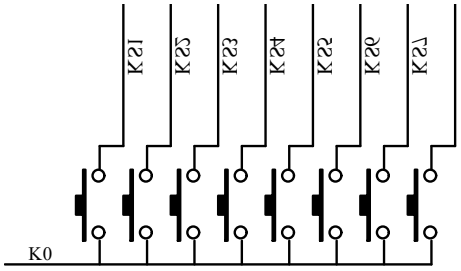


Chart3

Key scan data stock register as chart4, first send read key instruction, start to read key data BYTE1-BYTE4, read data from low, when press the key corresponding K and KS pin, the corresponding bit is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
X	X	X	K0	X	X	X	K0	
KS1				KS2				BYTE1
KS3				KS4				BYTE2
KS5				KS6				BYTE3
KS7				KS8				BYTE4

Chart4

Note:1, TM1629C could read at most 4 byte.

2, Read data just from BYTE1-BYTE4, cannot overleap.

3. Key combination just is the same KS, different K pin can combine to combination; same K with different K pin cannot combine.

B7	B6	instruction
0	1	Data instruction se
1	0	Display control data se
1	1	Address instruction set

If STB is high level when transmit instruction or data, serial communication is initialized, and the sending data or instruction is unvalid.(previous data or instruction is still valid.)

6.1 data instruction set

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	description
0	1	irrelevantterm, input 0				0	0	Data read&writ mode set	Write data to display registe
0	1					1	0		Read key scan dat
0	1				0			Auto-add address mode	Auto-add address
0	1				1				Fixed address
0	1			0				Test mode(inner use	mal mode
0	1			1					Test mode

6.2 address instruction set

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	irrelevantterm, input 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

The instruction is to set display register address.

If address set is 10H or hghter, the data would be ignored, till the valid address is se

When poweron, address fault is 00H

6.3 Display control:

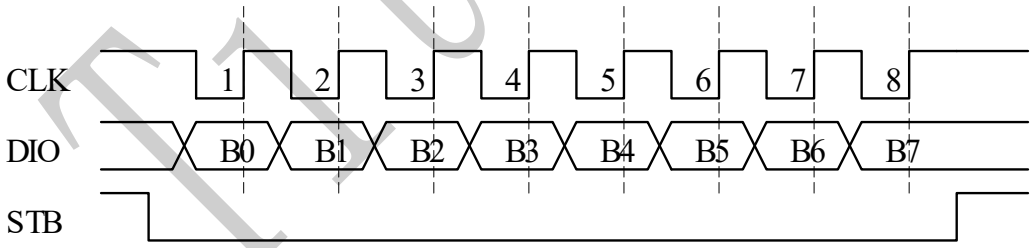
MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	description
1	0	Irrelevant term, input 0			0	0	0	Flatness quantity se	Set pulse width is 1/16
1	0				0	0	1		Set pulse width is 2/16
1	0				0	1	0		Set pulse width is 4/16
1	0				0	1	1		Set pulse width is 10/16
1	0				1	0	0		Set pulse width is 11/16
1	0				1	0	1		Set pulse width is 12/16
1	0				1	1	0		Set pulse width is 13/16
1	0				1	1	1		Set pulse width is 14/16
1	0			0				Display turn on/off set	play turn off
1	0			1					play turn on

7. serial data transmit type:

Read and receive a BIT in the clock up along the operation.

7. 1 data receive(write data)



图（5）

7. 2 2 data read

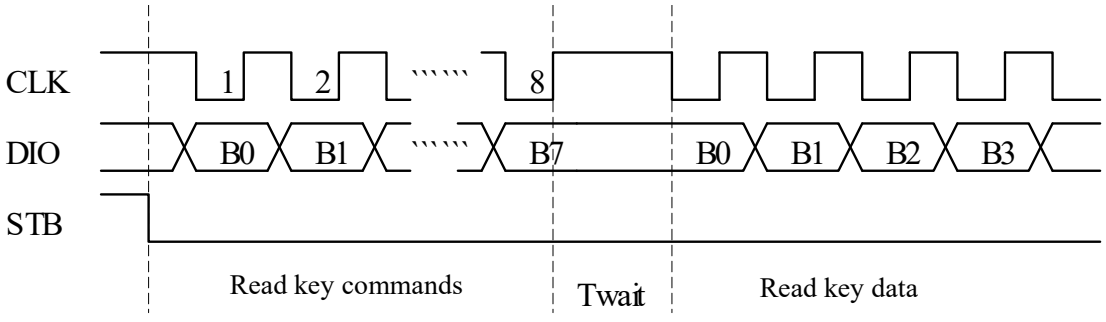


Chart6

Note: when read data, Twait(min is 1μS) is demand to set instruction from 8th rising edge of CLK to read data of CLK falling edge.

8. display and key press:

1. driver common cathode nixie

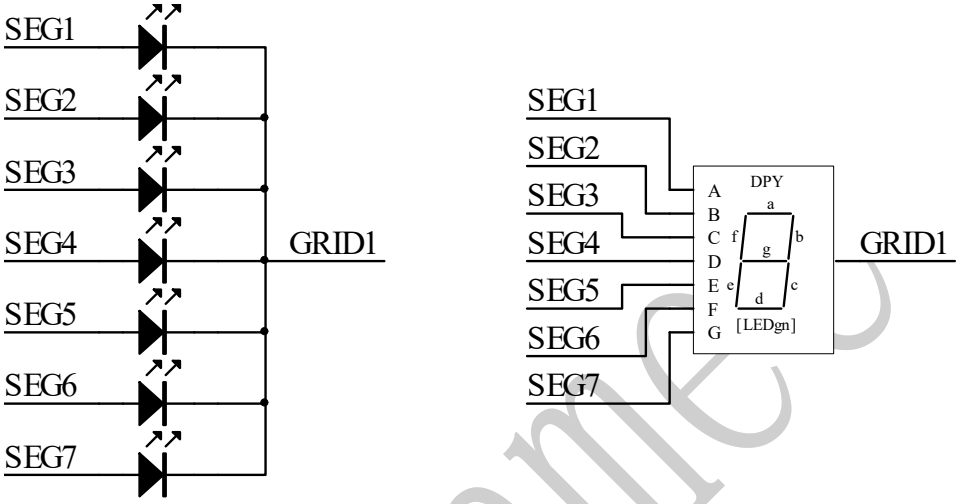


Chart7

Chart7 showed common cathode nixie tube connection, if the nixie tube display"0", the SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 should be high level, SEG7 should be low level when GRID1 is low level. Please check chart2 to display address chart, just input 3FH into 0H address unit that could let nixie tube display "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

2. driver common anode

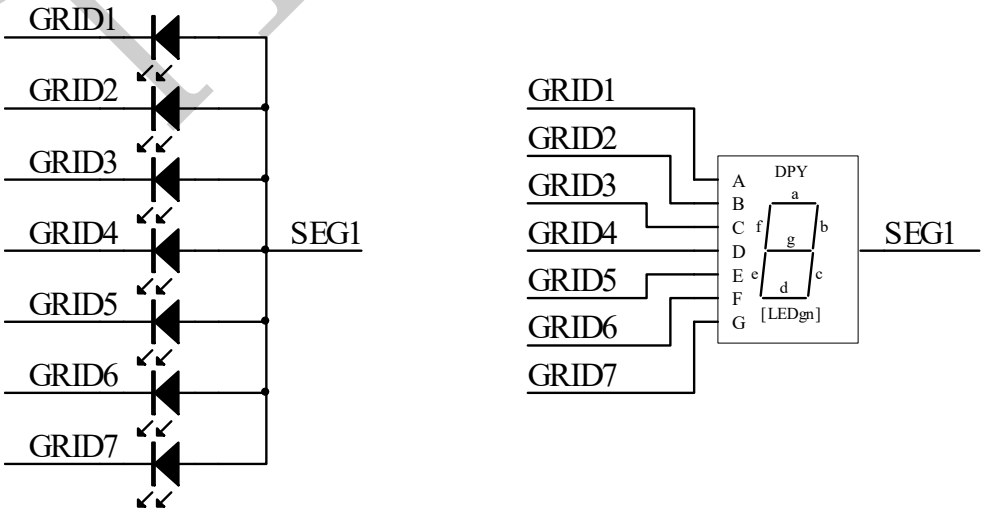


Chart8

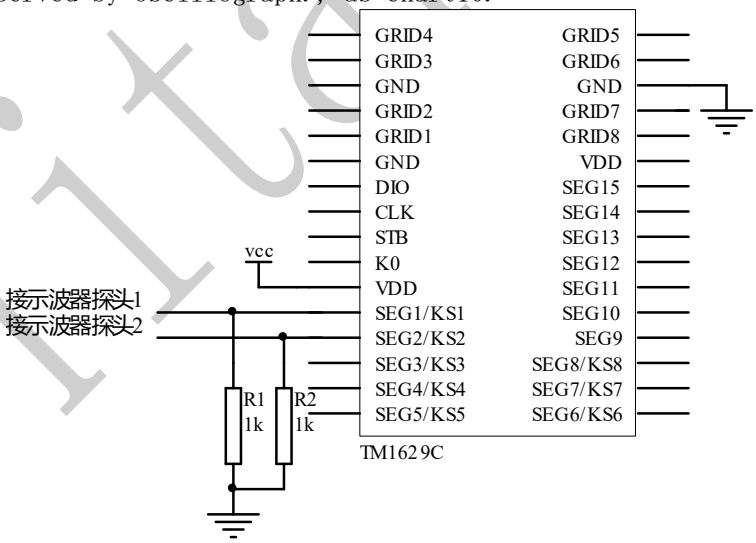
Chart8 display common anode nixie tube connection chart, if want the tube display”0”, SEG1 should be high level when GRID1, GRID2, GRID3, GRID4, GRID5, GRID6 is low level. If want SEG1 is low level when GRID7 is low level, please write data 01H to address unit 00H, 02H, 04H, 06H, 08H, 0AH. The rest address unit is written data 00H.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0AH
0	0	0	0	0	0	0	0	0CH
B7	B6	B5	B4	B3	B2	B1	B0	

Note: SEG1-11 is P-channel open-drain output, GRID1-7 is N-channel open-drain output, during use, SEG1-11 just could connect LED anode, GRID just could connect LED cathode.

（2） key.

Key scan is auto-completed by TM1629C, user just follow timing to read key value. 2 display period is demand to complete a key scan. A period need about T=8x500US , If press 2 different key at 8MS, the twice read key value just is the first press key’s value As chart9, output key scan wave of SEG1/KS1and SEG2/KS2 observed by oscillograph., as chart10.



Chart（9）

SEGN/KSN wave at IC keyboard scan:

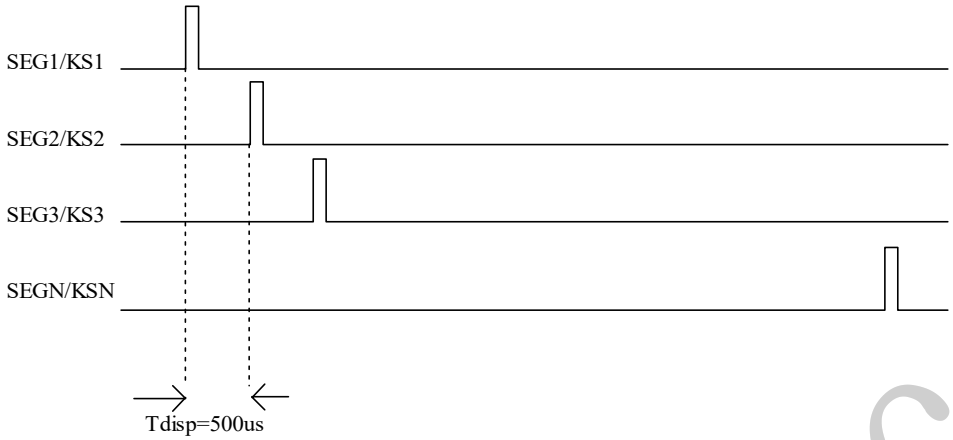
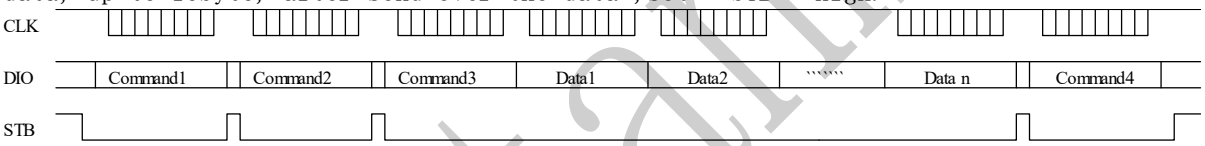


Chart (10)

Tdisp is related with oscillation frequency of IC work, 500US just for reference, please confirm by actual measurement.

9. 1 address-add mode

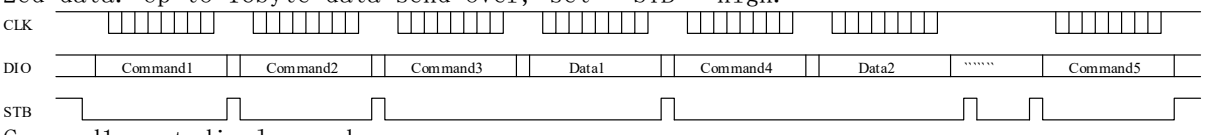
use address auto-add1 mode, set address actually is set the start address for stock data flow of transmit. After send over start address instruction byte, "STB" don't demand set high to transmit data, up to 16byte, after send over the data ,set "STB" high.



Command1: set display mode
Command2: set data instruction
Command3:set display address
Data1～ n: transmit display data to Command3 address and the next address (up to 16 bytes)
Command4: display control instruction

9. 2 fixed address mode

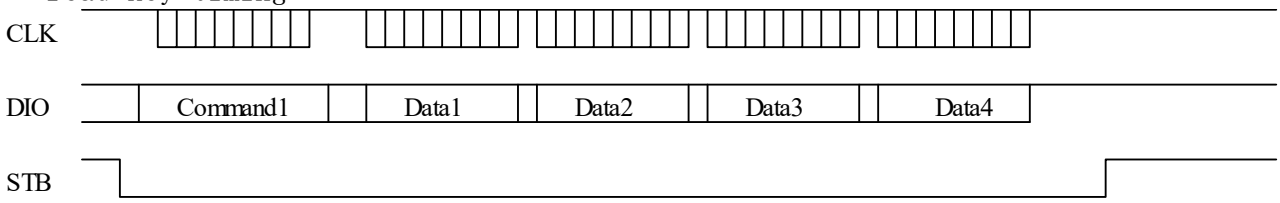
use fixed address mode, set address actually is set stock address for sending 1BYTE data. After send over, "STB"
don't demand set high, then send 1byte DATA. After all data send over, set"STB" high. Then set the stock address for
2ed data. Up to 16byte data send over, set "STB" high.



Command1: set display mode
Command2: set data instruction
Command3:set display address1
Data1: transmit display data1 to Command3 address

Command4: set display address2
Data2: transmit display data2 to Command4 address
Command5: display control instruction

9. 3 read key timing



Command1: set display mode
Data1～4:read key data

9. 4 procedure design flow chart

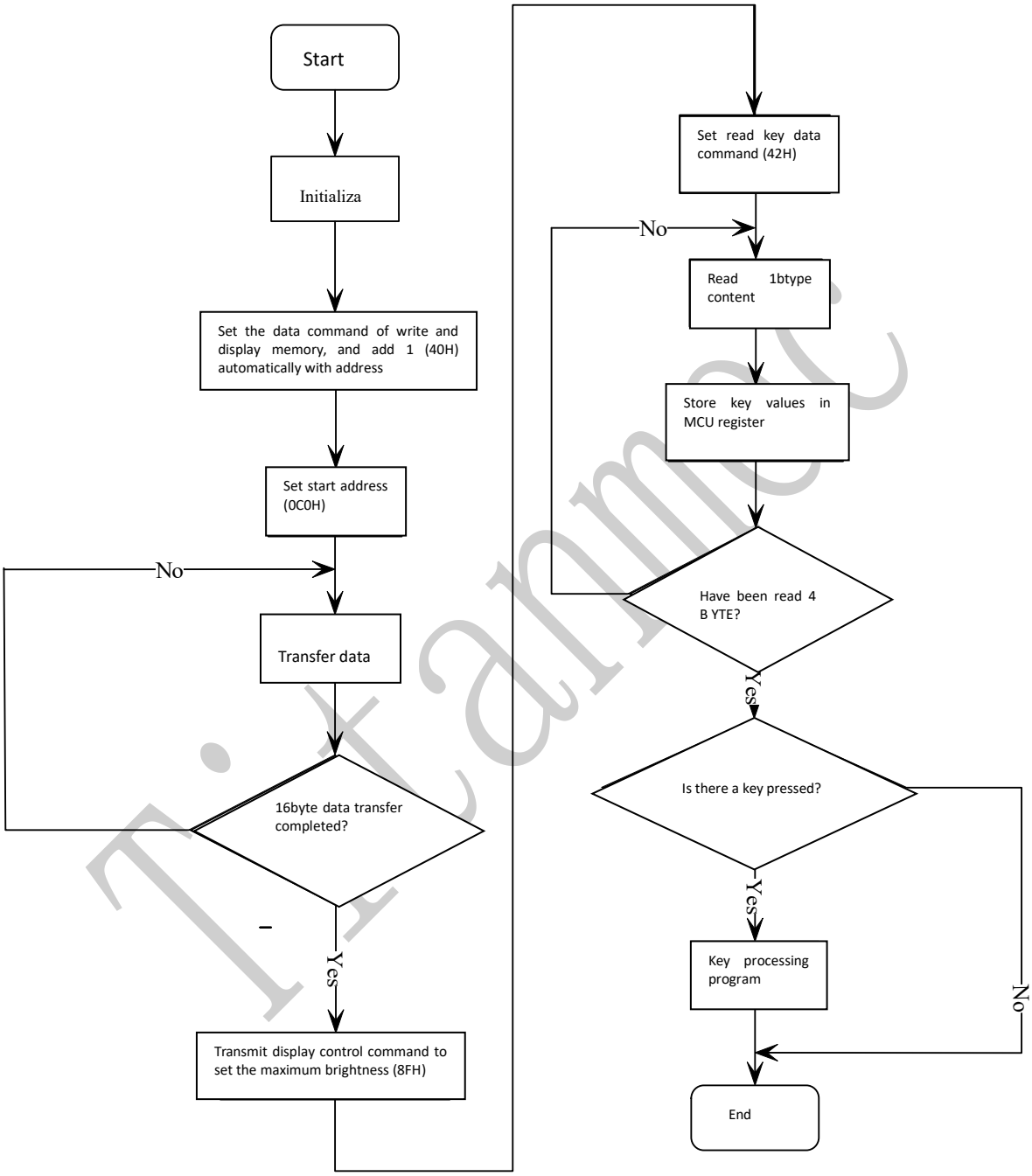
Use address auto-add 1 procedure design flow chart

9. 4-2

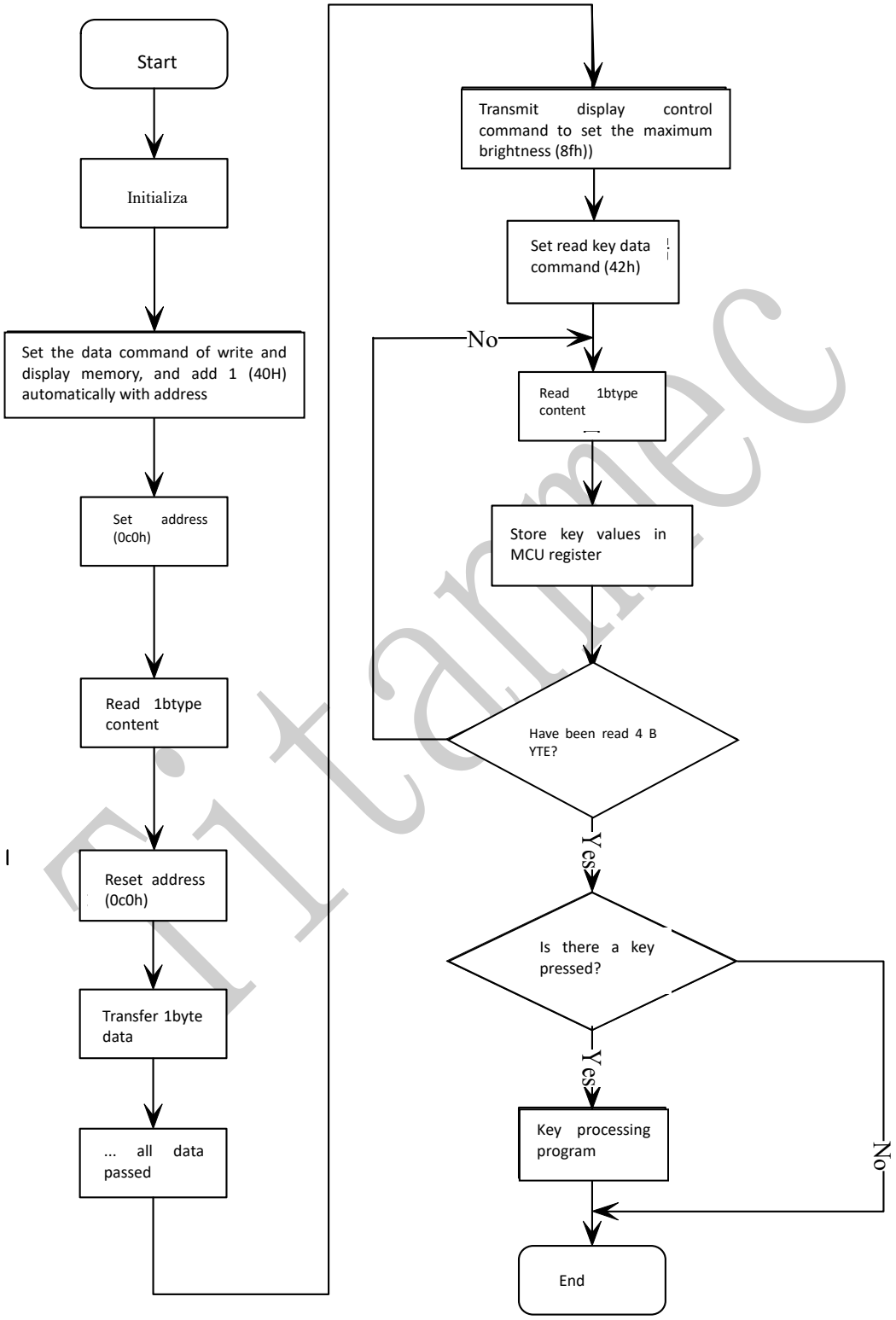
Use fixed address procedure design flow chart

（4）The flow chart of program design with address auto plus one and fixed address mode is as follows

The flow chart of program design with automatic address plus one is as follows

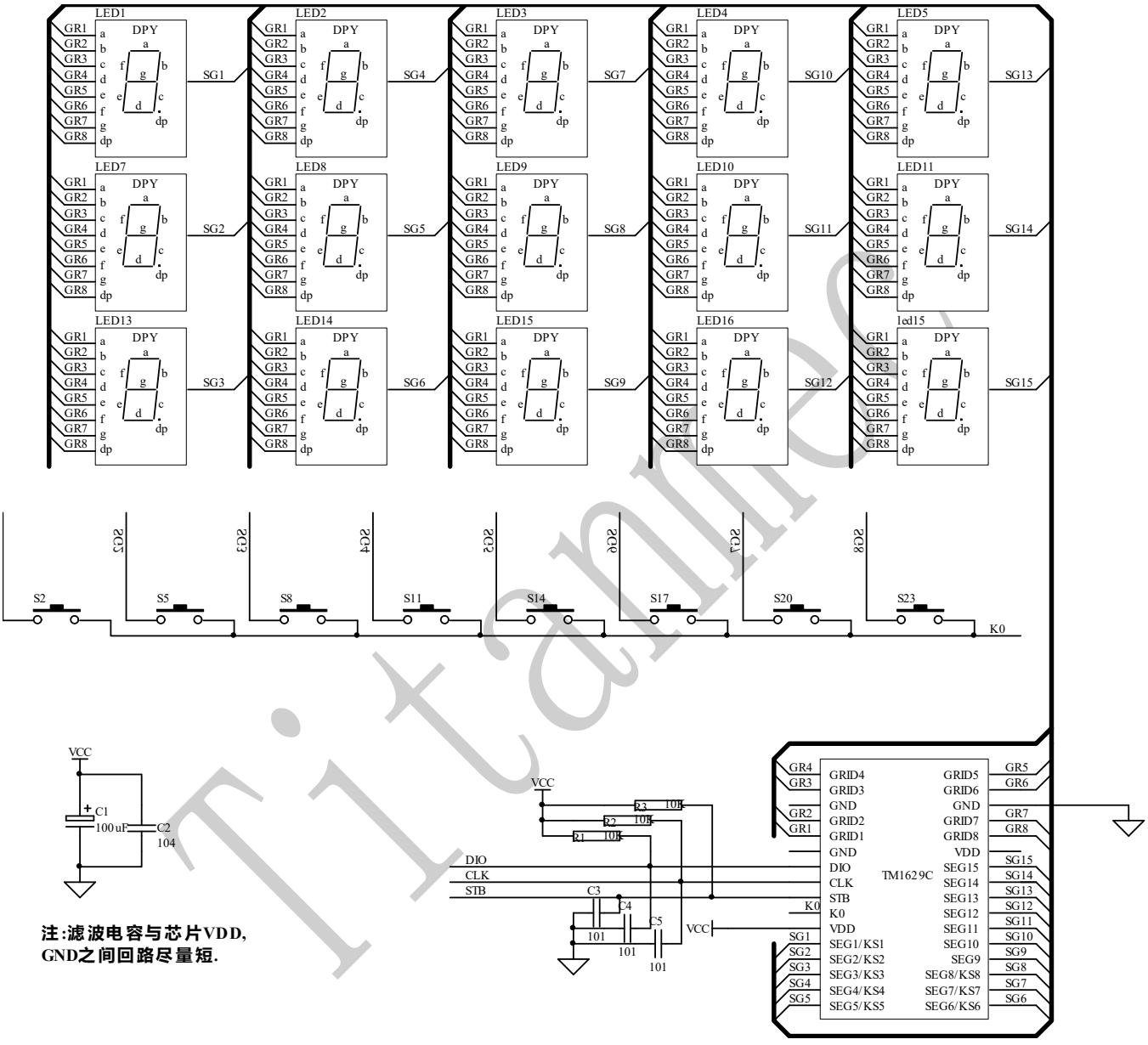


Flow chart of program design with fixed address:



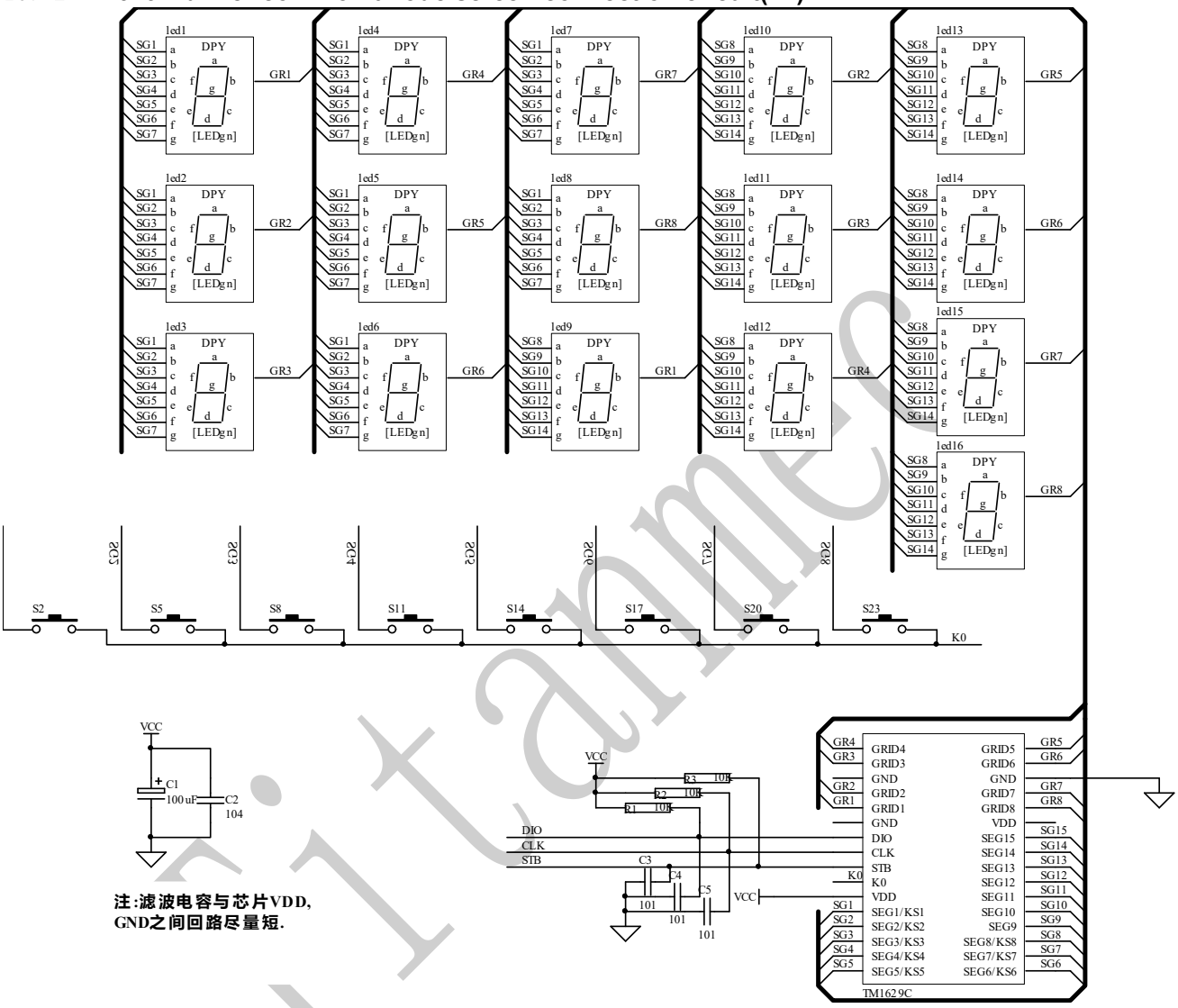
10. application circuit

10.1 TM1629C driver common cathode screen connection circuit(16)



Chart（16）

10. 2TM1629C driver common anode screen connection circuit(17)



Chart（17）

Note: 1. filter capacity between VDD and GND please near to TM1629C to enhance filter effort.

2. The 3 unit 100P capacity connect DIO, CLK and STB could decrease disturb for communication port.

3. Because blue light nixie tube breakover voltage drop about 3V, therefore TM1629C should choice 5V.

十一、 Electric Parameter

Limit parameter(Ta = 25℃, Vss = 0 V)

Parameter	Symbol	Range	uni
Logic power voltage	VDD	-0.5 ～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
LED Seg driver output voltage	IO1	-50	mA
LED Grid driver output current	IO2	+200	mA
Power consumption	PD	400	mW
Work temperature	Topt	-40 ～ +85	℃
Stock temperature	Tstg	-65 ～+150	℃

Normal work range (Vss = 0 V)

Parameter	Symbol	Min	Typical	Max	Unit	Text condition
Logic power voltage	VDD		5		V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

Electric Feature (VDD = 4.5 ～ 5.5 V, Vss = 0 V

Parameter	Symbol	Min	Typical	Max	Unit	Text condition
High level output current	Ioh1	-20	-25	-40	mA	Seg1~Seg11, Vo = vdd-2V
	Ioh2	-20	-30	-50	mA	Seg1~Seg11, Vo = vdd-3V

Low level output current	IOL1	80	140	-	mA	Grid1~Grid6 Vo=0.3V
Low level output current	Idout	4	-	-	mA	VO = 0.4V, dout
High level output current tolerance	Itolsg	-	-	5	%	VO = VDD - 3V, Seg1～Seg11
Output falling resistance	RL		10		KΩ	K1~K3
Input current	II	-	-	±1	μA	VI = VDD / VSS
High level input voltage	VIH	0.7 VDD	-		V	CLK, DIN, STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK, DIN, STB
Delay voltage	VH	-	0.35	-	V	CLK, DIN, STB
Positive current consumption	IDDdyn	-	-	5	mA	No load, display turn-of

Turn on/off feature (VDD = 4.5 ～ 5.5 V)

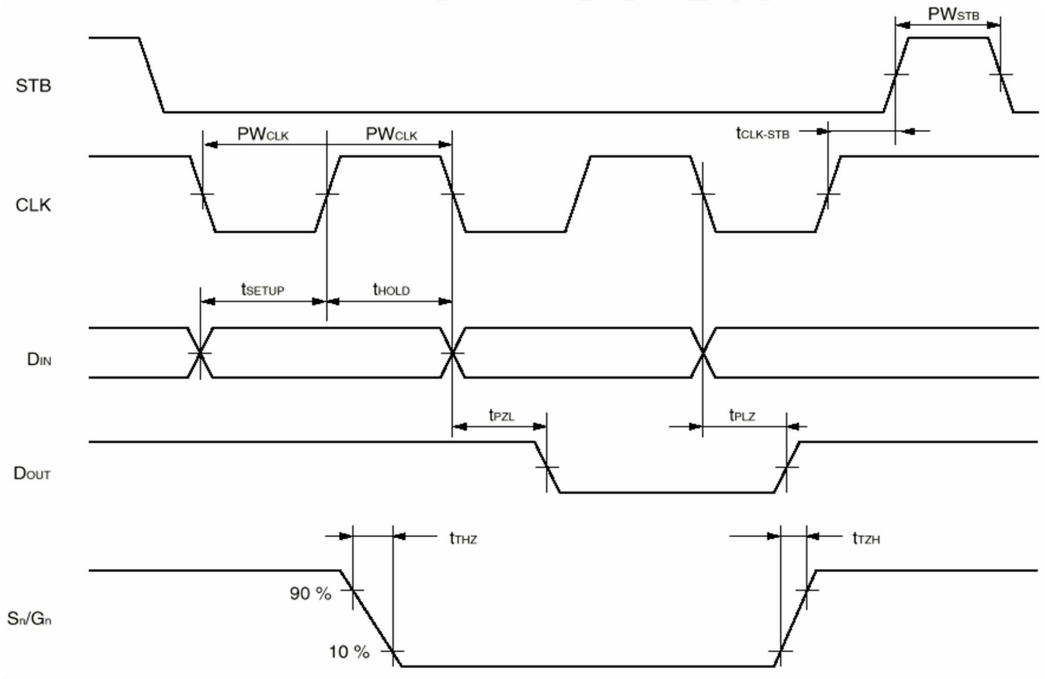
Parameter	Symbol	Min	Typical	Max	Unit	Text condition	
Oscillation frequency	fosc	-	500	-	KHz	R = 16.5 KΩ	
Transmit delay time	tPLZ	-	-	300	ns	CLK → DOUT	
	tPZL	-	-	100	Ns	CL = 15pF, RL = 10K Ω	
Rising time	TTZH 1	-	-	2	μs	CL = 300p F	Seg1～Seg11
	TTZH 2	-	-	0.5	μs		Grid1～Grid4 Seg12/Grid7～ Seg14/Grid5
Falling time	TTHZ	-	-	120	μs	CL = 300pF, Seg N, Grid N	

Max clock frequency	Fmax	1	-	-	MHz	Duty ratio 50
Input capacity	CI	-	-	15	pF	-

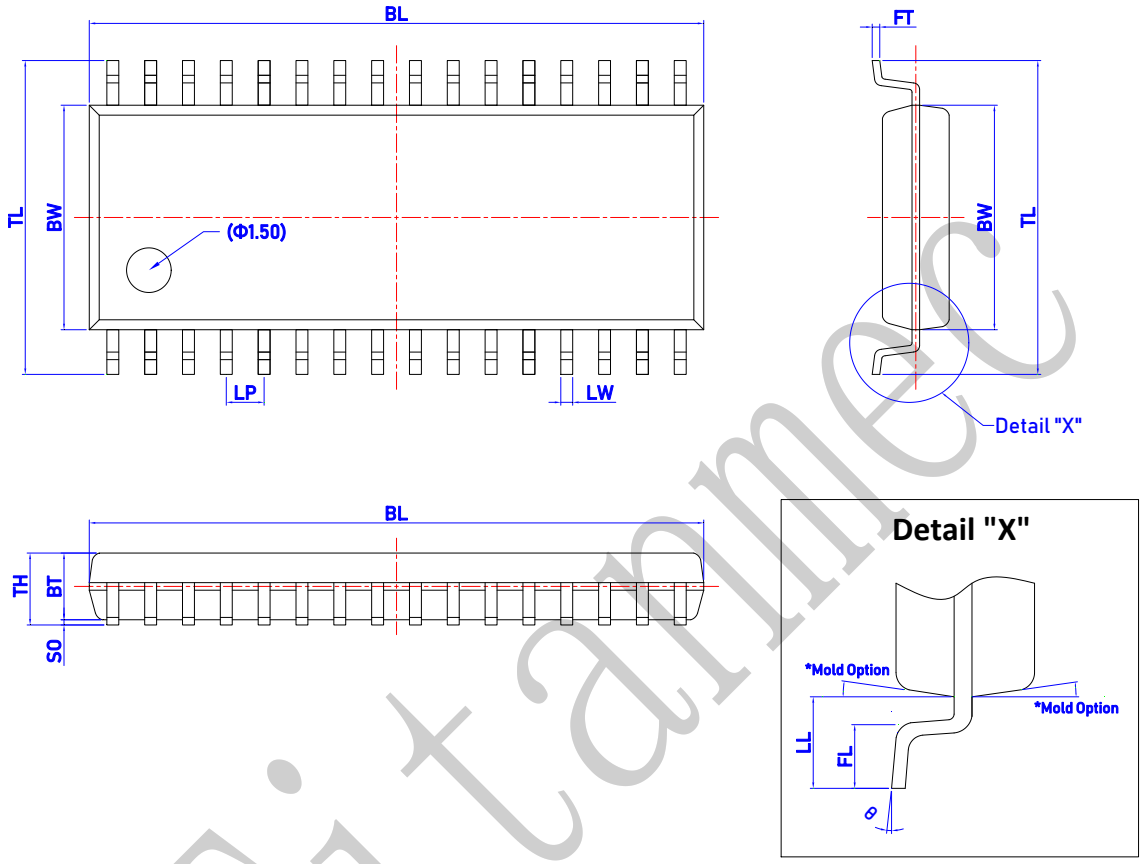
Timing Feature（VDD = 4.5 ～ 5.5 V）

Parameter	Symbol	Min	Typical	Max	Uni	Test condition
Clock pulse width	PWCLK	400	-	-	ns	-
Gate pulse width	PWSTB	1	-	-	μs	-
Data building time	TSETUP	100	-	-	ns	-
Data keep time	THOLD	100	-	-	ns	-
CLK →STB time	TCLK STB	1	-	-	μs	CLK↑→STB↑
Waiting time	TWAIT	1	-	-	μs	CLK↑→CLK↓

Timing wave chart:



12、 package (SOP32-300)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	20.73 (20.63) 20.53	7.64 (7.54) 7.44	10.60 (10.40) 10.20	0.400 TYP	1.270 TYP	0.250 (0.200) 0.170	2.34 (2.24) 2.14	0.250 (0.175) 0.100	2.490 Max.	1.60 (1.50) 1.40	0.95 (0.75) 0.55	8 (4) 0

- All specs and applications shown above subject to change without prior notice.
  (以上电路及规格仅供参考,如本公司进行修正，恕不另行通知。)