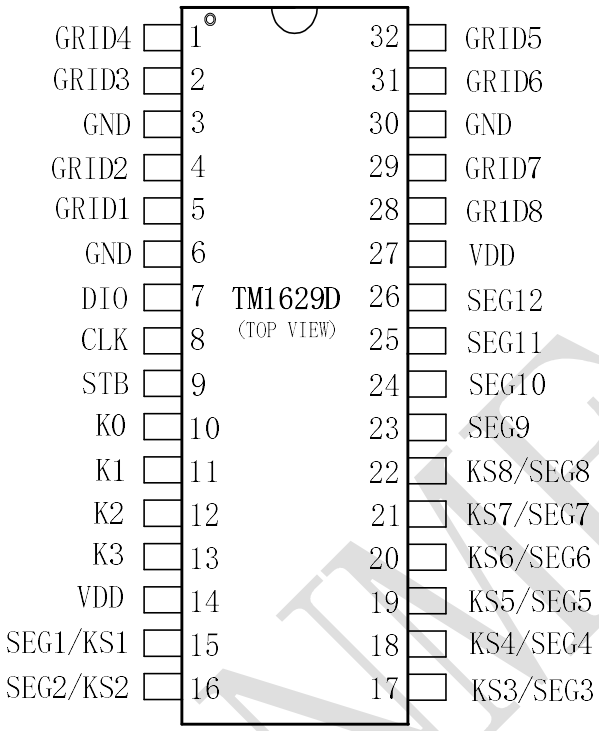
I. Overview

TM1629D is a kind of LED driver control IC with keyboard scan interface. The internal integration of MCU digital interface, data latch, LED driver, keyboard scanning circuit. This product has reliable quality, good stability and strong anti-interference ability. It is mainly suitable for home appliances (intelligent water heater, microwave oven, washing machine, air conditioner, induction cooker), set top box, electronic scale, smart meter and other digital tube or LED display equipment.

II. Characteristic description

- Using CMOS technology
- Display mode 12 segments × 8 bits
- Maximum support matrix key 8 × 4
- Brightness adjustment circuit (duty cycle 8 levels adjustable)
- Serial interface (CLK, STB, DIO)
- Oscillation mode: built in RC oscillation
- Built in power on reset circuit
- Built in data latch circuit
- Strong anti-interference ability
- Built in optimization circuit for LED reverse bias leakage leading to dark and bright problem
- Package form: SOP32

II. Pin definition



IV. Pin function description

Symbol	Pin name	Pin number	Explain
DIO	Data output input	7	Input serial data at the rising edge of the clock, starting from the low bit. The serial data is output along the clock down, starting from the low position. When the output is n-tube open drain output, external need to connect 1-10k Ω pull-up resistor to VCC.
CLK	Clock input	8	Read serial data on the rising edge and output data along the descent edge.
STB	Selected films	9	Initialize the serial interface on the descent edge, and then wait for the receive command. STB is the first byte after the low as the instruction, and when processing the instruction, the current other processing is terminated. When STB is high, CLK is ignored.

K0～K3	Key scan data input	10～13	The data of the input pin is locked after the display period is finished, and the 7.3k pull-down resistance is built in.
SEG1/KS1～ SEG8/KS8	Output (segment)	15～22	The output of section (also used as key scanning), p-tube open leakage output, built-in 3.6k pull-down resistance.
SEG9～SEG12	Output (segment)	23～26	Section output, p-tube open drain output, built-in 3.6k pull-down resistor.
GRID1～GRID2 GRID3～GRID4 GRID5～GRID6 GRID7～GRID8	Output (bit)	5～4 2～1 32～31 29～28	Bit output, n-tube open drain output, built-in 2.8k pull-up resistor.
VDD	Logic power supply	27,14	Connect the power supply.
GND	Logical place	3,6 30	Ground the system.

▲Note: the DIO port output data is n-tube open drain output, and external 1K-10K pull-up resistor is needed when reading key. The company recommends 10K pull-up resistor. DIO controls the action of N-tube at the falling edge of the clock. At this time, the reading is unstable, and the reading is stable at the rising edge.

V. Instructions:

The command is used to set the display mode and the status of the LED driver.

The first byte entered by DIN after the falling edge of STB is used as the instruction. After decoding, the highest B7 and B6 bits are selected to distinguish different instructions.

B7	B6	Instructions
0	1	Data command settings
1	0	Display control command settings
1	1	Address command settings

If STB is set to high level during command or data transmission. Serial communication is initialized and the instruction or data being transmitted is invalid (the instruction or data previously transmitted remains valid).

（1） Data command settings:

This instruction is used to set the data write and read, B1 and B0 bits are not allowed to set 01 or 11.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Explain	Explain
0	1	For irrelevant items, fill in 0.				0	0	Data read/write mode setting	Write data to display register
0	1					1	0		Read key scan data
0	1				0			Address increase mode setting	Automatic address increase
0	1				1				Fixed address
0	1			0				Mode setting	Normal mode

（2） Display control command settings:

This command is used to set the switch of display and adjust the brightness of display. There are 8 levels of brightness to choose from.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Explain
1	0	For irrelevant items, fill in 0.			0	0	0	Extinction quantity setting	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch settings	Display off
1	0			1					Display on

（3） Address command settings:

This instruction is used to set the address of the display register. The maximum effective address is 16 bits (C0H-CFH). If the address is set to D0H or higher, the data is ignored until the effective address is set. When power on, the address is set to C0H by default.

MSB							LSB	
B7	B6	B5	B4	B3	B2	B1	B0	display address
1	1	For irrelevant items, fill in 0.		0	0	0	0	C0H
1	1			0	0	0	1	C1H
1	1			0	0	1	0	C2H
1	1			0	0	1	1	C3H
1	1			0	1	0	0	C4H
1	1			0	1	0	1	C5H
1	1			0	1	1	0	C6H
1	1			0	1	1	1	C7H
1	1			1	0	0	0	C8H
1	1			1	0	0	1	C9H
1	1			1	0	1	0	CAH
1	1			1	0	1	1	CBH
1	1			1	1	0	0	CCH
1	1			1	1	0	1	CDH
1	1			1	1	1	0	CEH
1	1			1	1	1	1	CFH

VI. Display register address

The register stores the data transmitted from external devices to tm1629d through the serial interface. The address is a 16 byte unit from c0h-cfh, which corresponds to the LED lights connected to the chip SGE and grid pins respectively. The allocation is as follows:

When writing LED display data, operate from low bit to high bit of display address and from low bit to high bit of data byte.

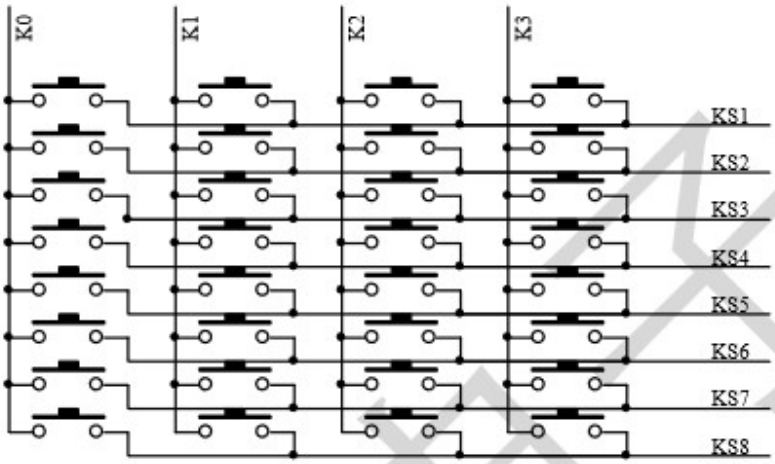
SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	X	X	X	X	
xxHL(Low four bits)				xxHU(High four bits)				xxHL(Low four bits)				xxHU(High four bits)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
C0HL				C0HU				C1HL				C1HU				**GRID1**
C2HL				C2HU				C3HL				C3HU				**GRID2**
C4HL				C4HU				C5HL				C5HU				**GRID3**
C6HL				C6HU				C7HL				C7HU				**GRID4**
C8HL				C8HU				C9HL				C9HU				**GRID5**
CAHL				CAHU				CBHL				CBHU				**GRID6**
CCHL				CCHU				CDHL				CDHU				**GRID7**
CEHL				CEHU				CFHL				CFHU				**GRID8**

Figure(2)

▲Note: the value stored in the chip display register at the moment of power on may be random and uncertain. At this time, if the customer directly sends the open screen command, the display garbled code may appear. Therefore, our company suggests the customer to perform a power on reset operation on the display register, that is, after power on, write all data 0x00 to the 16 bit video memory address (C0H-CFH).

VII. Key scan and key scan data register:

The key scan matrix is 8 × 4 bit, as shown in figure (3)



The key scan data storage address is as follows. After the key read command is issued, the key data BYTE1—BYTE4 is read, and the read data is output from the low position. When the key corresponding to the K and KS pins of the chip is pressed, the bit bit in the corresponding byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K3	K2	K1	K0	K3	K2	K1	K0	
KS1				KS2				BYTE1
KS3				KS4				BYTE2
KS5				KS6				BYTE3
KS7				KS8				BYTE4

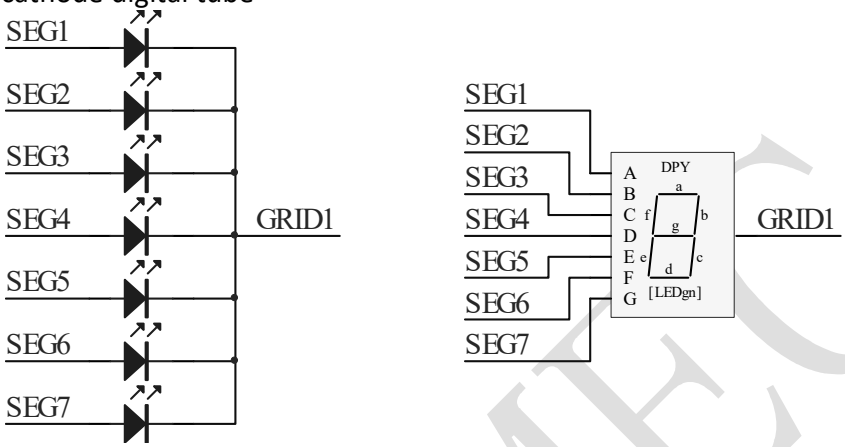
Figure(4)

▲**Note**:

1. TM1629D can read up to four bytes, and no more than one byte is allowed.
2. Read data bytes can only be read from BYTE1-BYTE4 in sequence, not across bytes. For example, when the key corresponding to K0 and KS8 on the hardware is pressed, if you want to read the key data, you must read the 7BIT bit of the fourth byte before you can read the data.

VIII. Display

1. Drive common cathode digital tube

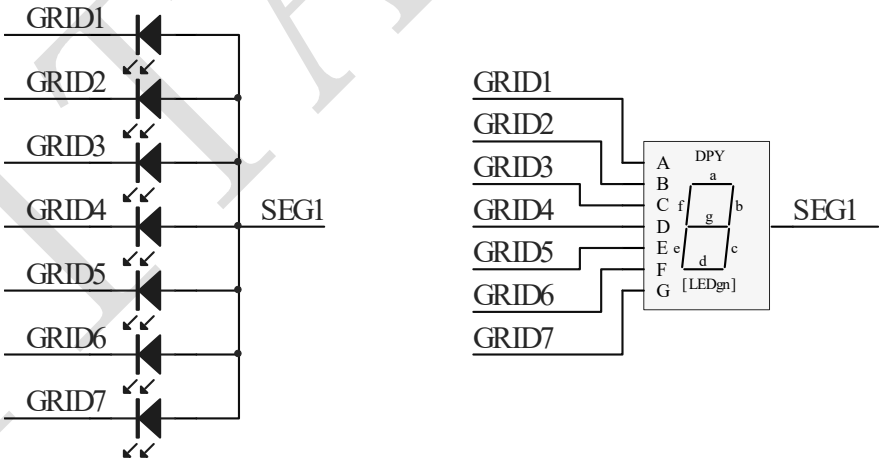


Figure(7)

Figure 7 shows the connection diagram of the common cathode digital tube. If you want the digital tube to display "0", you need to set SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 as high level and SEG7 as low level when GRID1 is low level, See figure (2) to display the address table. Just write data 3FH in 00h address unit to make the nixie tube display "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

2. Drive common positive digital tube:



Figure(8)

Figure 8 shows the connection diagram of the common positive digital tube. If you want the digital tube to display "0", you need to make seg1 high when GRID1, GRID2, GRID3, GRID4, GRID5 and GRID6 are low. When grid7 is low, let seg1 be low. Write data 01H to address units C0H, C2H, C4H, C6H, C8H and CAH respectively, and write data 00H to all other address units.

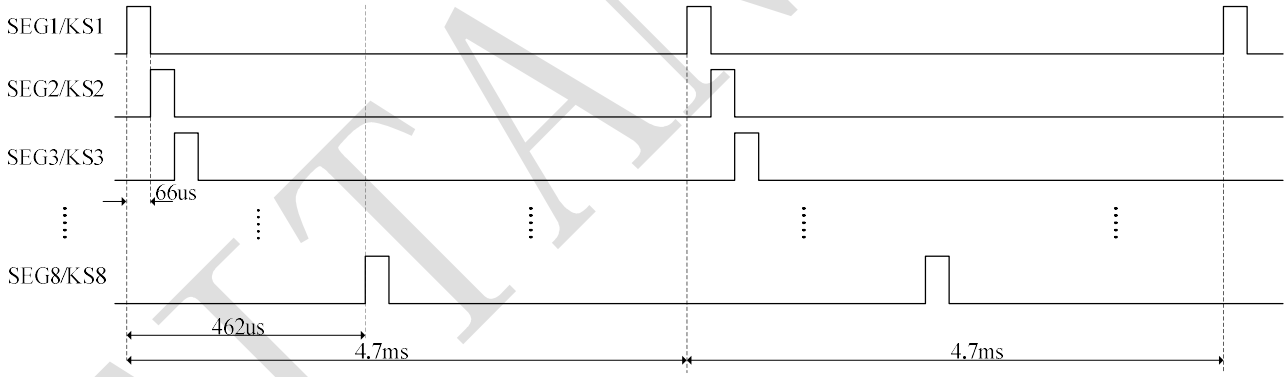
SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	C0H
0	0	0	0	0	0	0	1	C2H
0	0	0	0	0	0	0	1	C4H
0	0	0	0	0	0	0	1	C6H
0	0	0	0	0	0	0	1	C8H
0	0	0	0	0	0	0	1	CAH
0	0	0	0	0	0	0	0	CCH
B7	B6	B5	B4	B3	B2	B1	B0	

▲Note: SEG1-15 is p-tube open drain output, GRID1-8 is n-tube open drain output. In use, SEG1-15 can only be connected to the anode of the LED, GRID can only be connected to the cathode of the LED, not reversed.

IX. Press the key:

(1) Key scanning: the key scanning is automatically completed by TM1629D, which is not controlled by the user. The user only needs to read the key value according to the sequence. It takes one display cycle to complete a key scan, and one display cycle takes about t = 4.7ms. In 4.7ms, two different keys were pressed successively, and the key values read twice were the key values of the first key pressed.

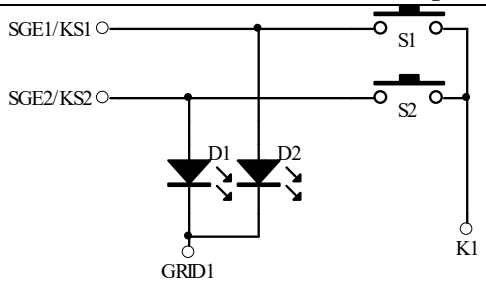
After the TM1629D is powered on, the waveform of SEG1/KS1-SEG8/KS8 is shown in figure (10)



Figure(10)

▲**Note:** one cycle time is related to the oscillation frequency of IC, and the oscillation frequency of each IC is not completely consistent. The above data are for reference only, subject to the actual measurement.

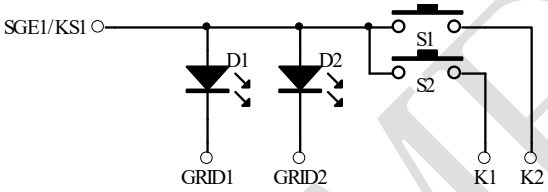
(2) Key reuse: the problem of composite key is abnormal: SEG1/KS1-SEG8/KS8 is display and key scan reuse. Take figure (12) as an example to show that D1 needs to be on and D2 needs to be off. It is necessary to set SEG1 to "0" and SEG2 to "1" state. If S1 and S2 are pressed at the same time, it is equivalent to SEG1 and SEG2 being short circuited. At this time, D1 and D2 are lit.



Figure(12)

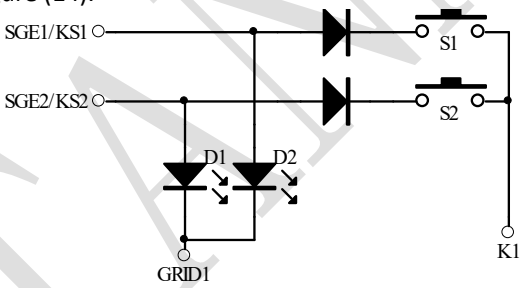
Solution:

1. On the hardware, the keys that need to be pressed at the same time can be set on different K lines, as shown in figure (13),



Figure(13)

2. The diode in series is shown in figure (14).



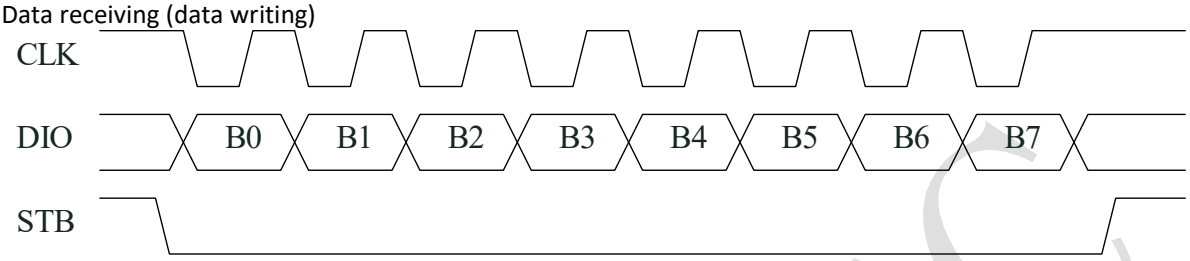
Figure(14)

▲**Note:** it is recommended to use different K keys of the same KS as composite keys.

X. Serial data transmission format

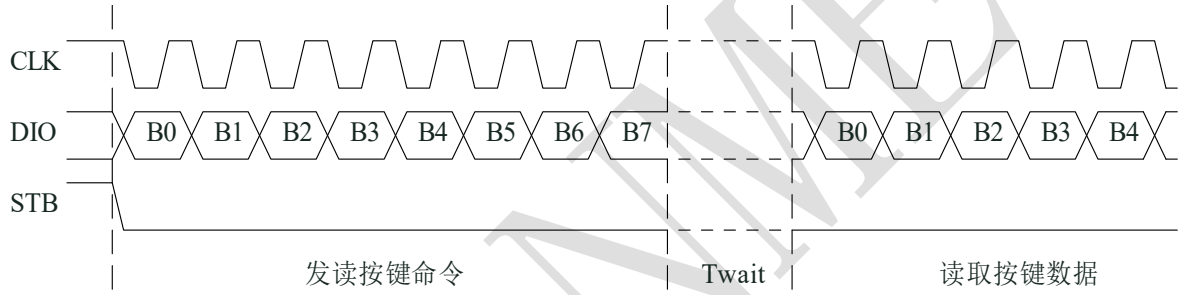
Read and receive 1 bit both operate on the rising edge of the clock

Data receiving (data writing)



Figure(5)

Data receiving (data reading)



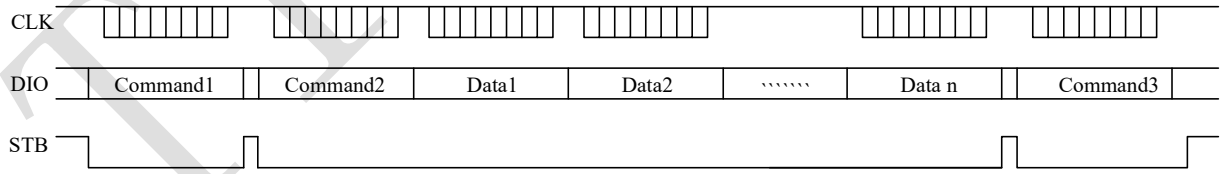
Figure(6)

▲Note: 1. When reading data, there is a waiting time twait (minimum 2 μ s) between setting instruction from the 8th rising edge of serial clock CLK and reading data from the falling edge of CLK. See the time sequence characteristic table for specific parameters.

XI. When applied, the transmission of serial data:

(1) Address increase mode

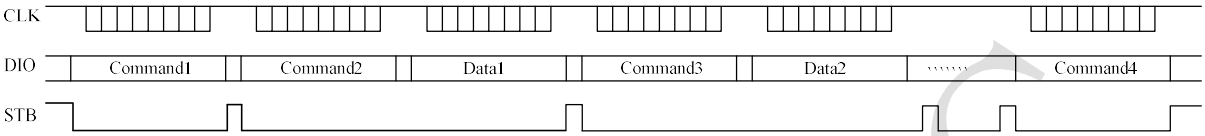
Using the mode of address auto plus 1, setting the address is actually setting the starting address of the data stream. After the start address command word is sent, "STB" does not need to be set high to transfer data immediately. At most, it is 16byte. After the data is transferred, "STB" is set high.



Command1: set data command
Command2: set display address
Data1～n: transmit the display data to the address of command2 and the following address (up to 16bytes)
Command3: display control command

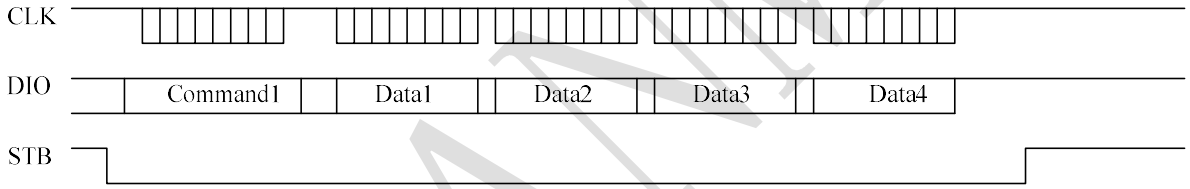
(2) Fixed address mode

Using the fixed address mode, setting the address is actually setting the address where the 1byte data to be transmitted is stored. After the address is sent, "STB" does not need to be set high, but 1BYTE data is transferred immediately, and "STB" is set high after data transmission. Then reset the address where the second data needs to be stored. After the 16BYTE data transmission is completed, set "STB" high.



Command1: set data command
Command2: set display address 1
Data1: transfer display data 1 to the address of command2
Command3: set display address 2
Data2: transfer display data 2 to the address of command3
Command4: display control command

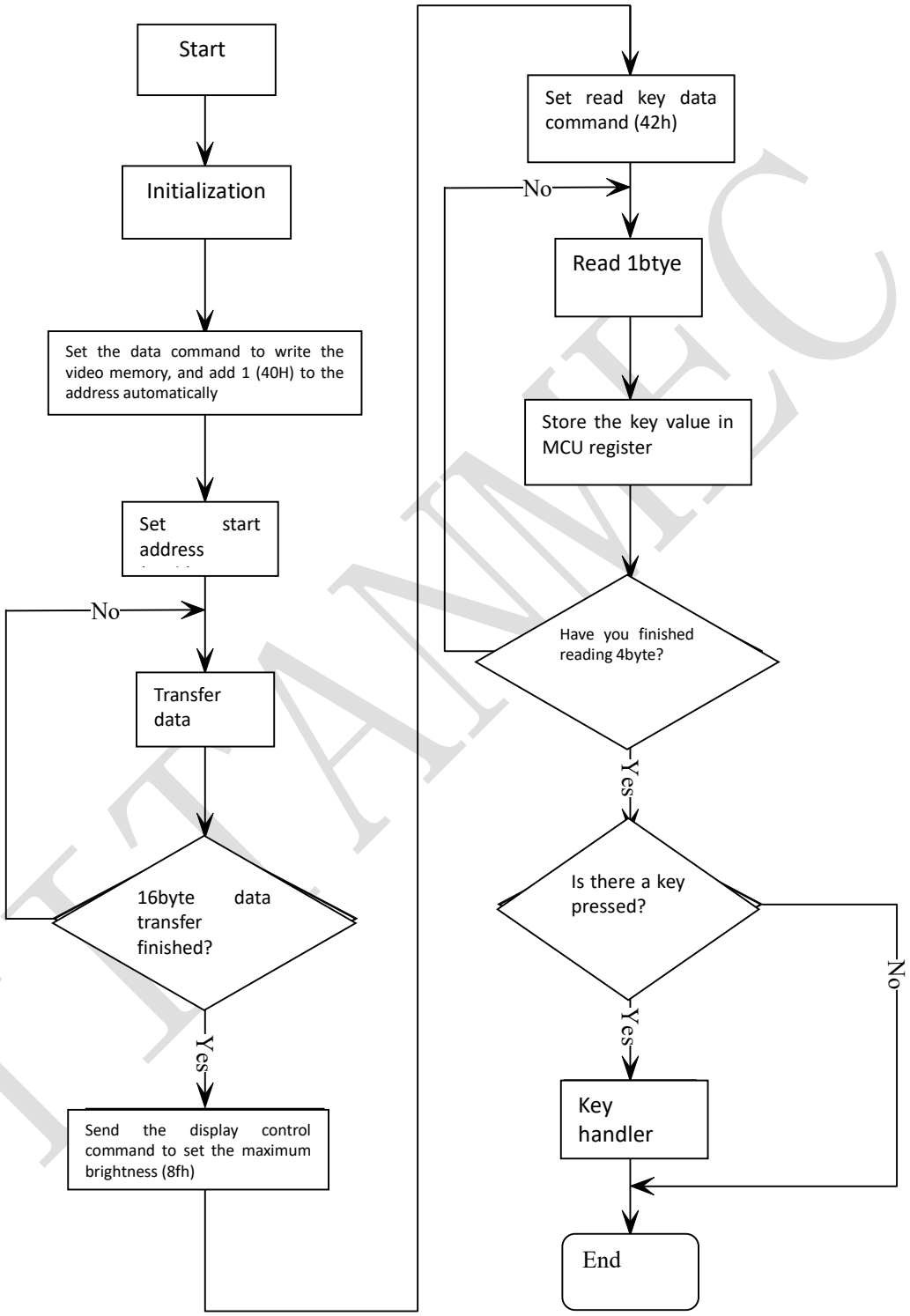
(3)Read key timing



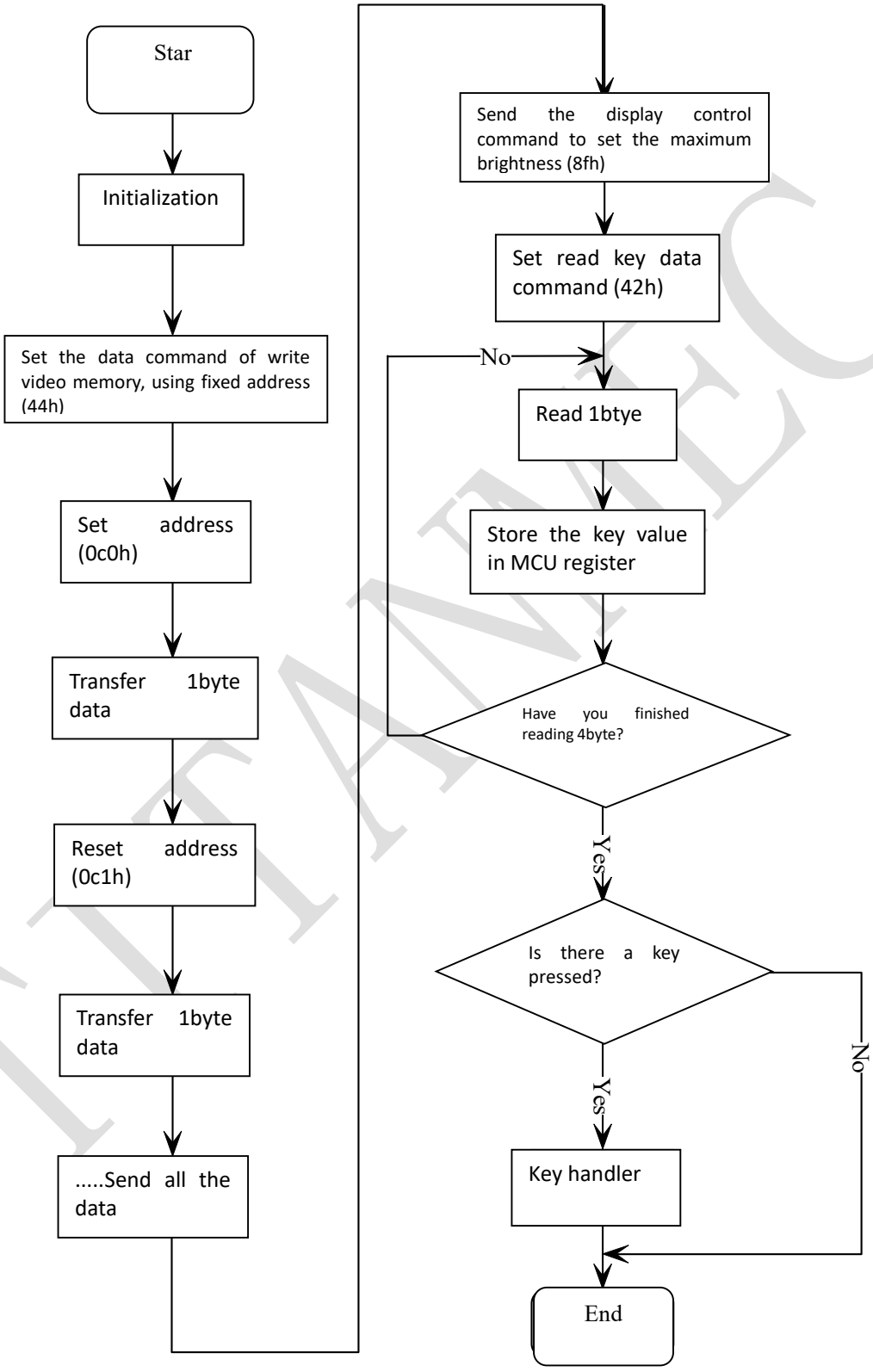
Command1: set read key command
Data1～4: read key data

(4) The flow chart of program design with address auto plus one and fixed address mode is as follows.

The flow chart is designed by adding one address automatically.

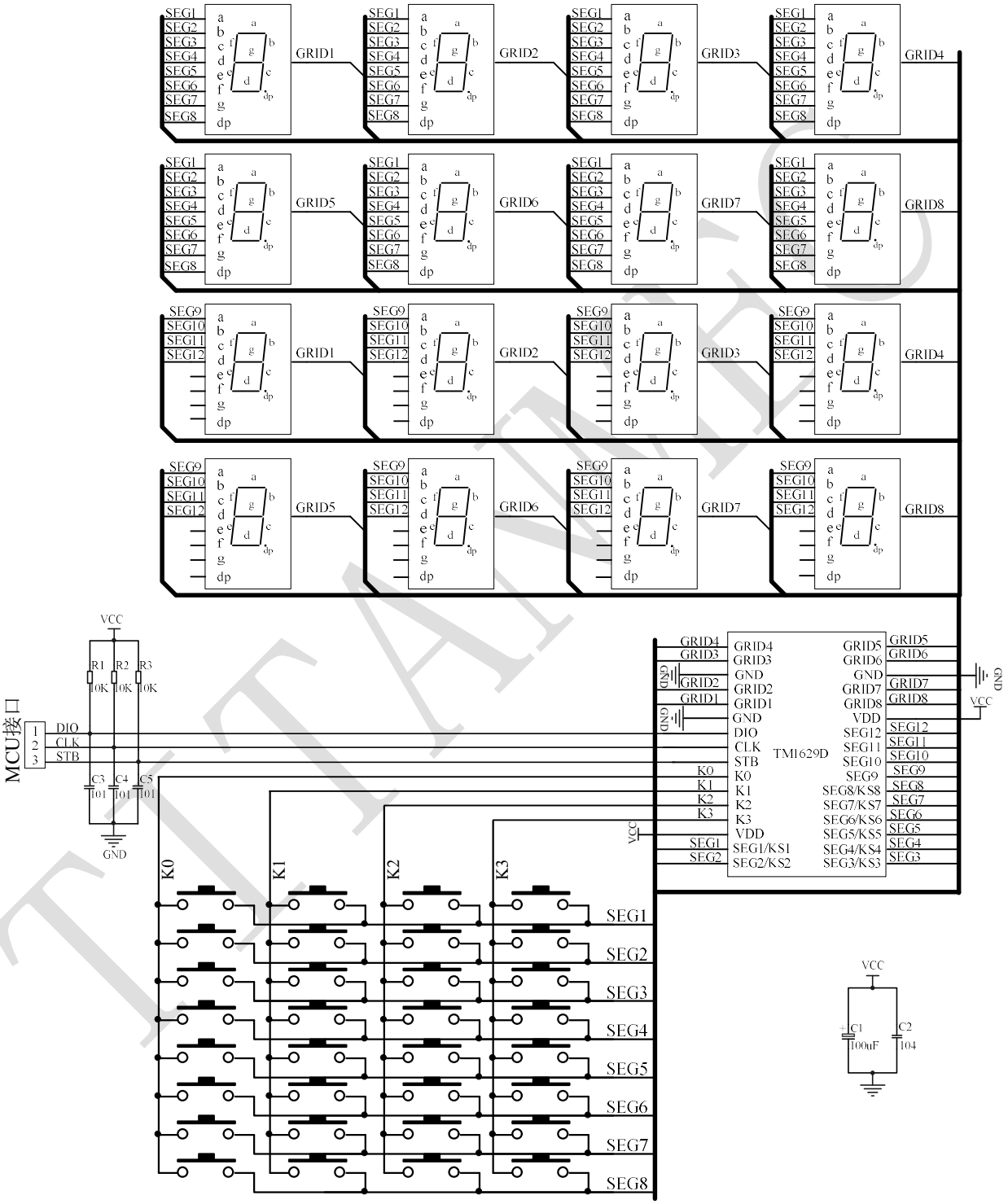


Programming flow with fixed address

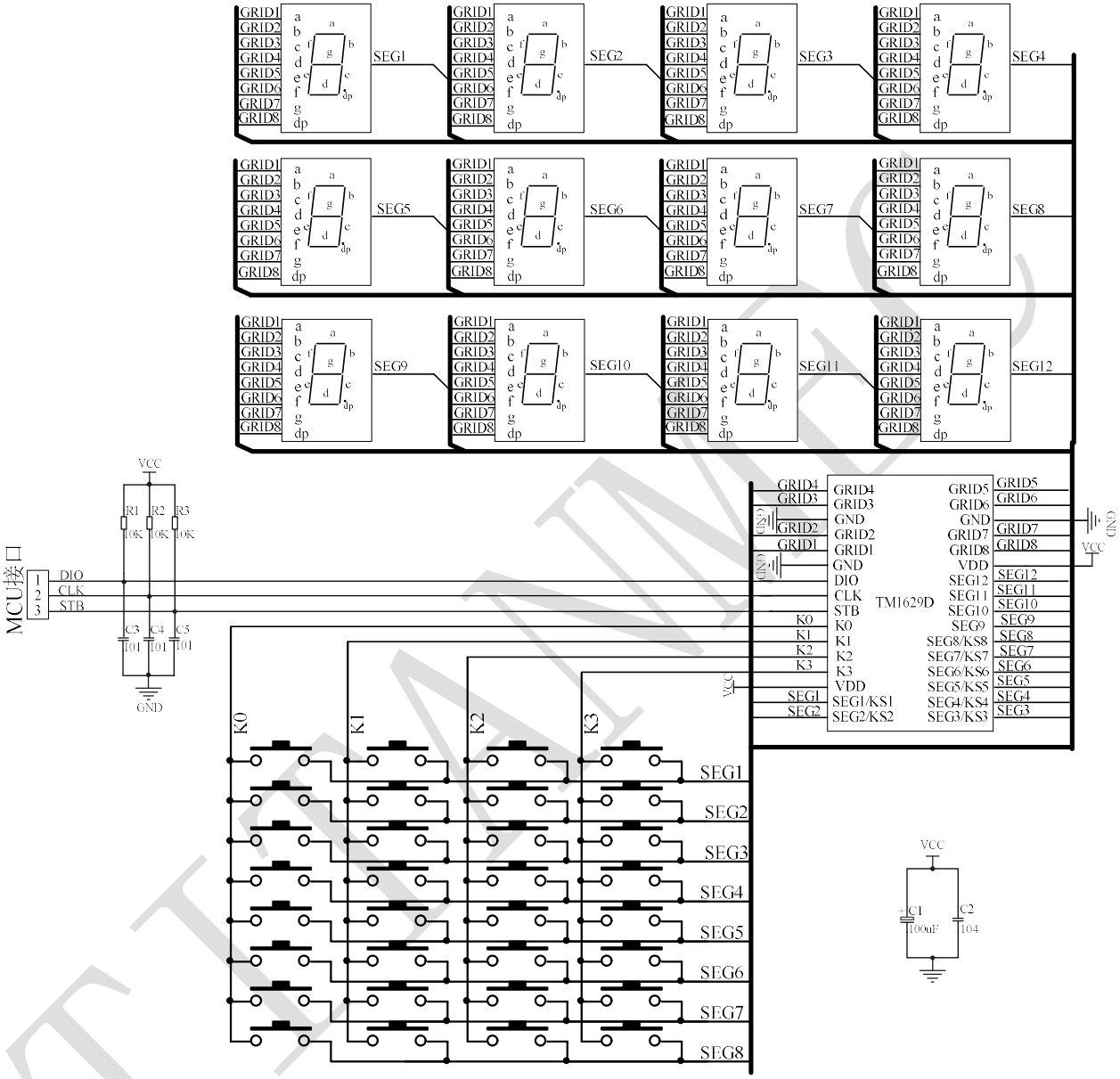


XI. Application circuit:

TM1629D Hardware circuit of driving common cathode digital screen



TM1629D Hardware circuit of driving common positive digital screen



▲Note:

1. The filter capacitor between VDD and GND should be placed close to TM1629D chip in PCB wiring to enhance the filtering effect.
2. Three 100p capacitors connected to DIO, CLK and STB communication ports can reduce the interference to communication ports.
3. Because the conduction voltage of blue LED is about 3V, the power supply of TM1629D should be 5V.

XII. Electrical parameters:

Limit parameter (Ta = 25℃, Vss = 0 V)

Parameter	Symbol	Scope	Unit
Logic supply voltage	VDD	-0.5 ～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
Led Seg drive output current	IO1	-50	mA
Led Grid drive output current	IO2	+200	mA
Power loss	PD	400	mW
Working temperature	Topt	-40 ～ +85	℃
Storage temperature	Tstg	-65 ～+150	℃

Normal operating range(Vss = 0 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions
Logic supply voltage	VDD	3	5	6	V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

Electrical characteristics(VDD = 4.5 ～ 5.5 V, Vss = 0 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions
High level output current	Ioh1	-20	-25	-40	mA	Seg1~Seg12, Vo = vdd-2V
	Ioh2	-20	-30	-50	mA	Seg1~Seg12, Vo = vdd-3V
Low level output current	IOL1	80	140	-	mA	Grid1~Grid8 Vo=0.3V

Low level output current	Idout	4	-	-	mA	Vo = 0.4V,dout
High level output current tolerance	Itolsg	-	-	5	%	Vo = VDD – 3V, Seg1～Seg12
Output pull-down resistance	RL		10		KΩ	K0
Input current	II	-	-	±1	μA	VI = VDD / VSS
High level input voltage	VIH	0.7 VDD	-		V	CLK,DIO,STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK,DIO,STB
Hysteresis voltage	VH	-	0.35	-	V	CLK,DIO,STB
Dynamic current loss	IDDdyn	-	-	5	mA	No load, display off

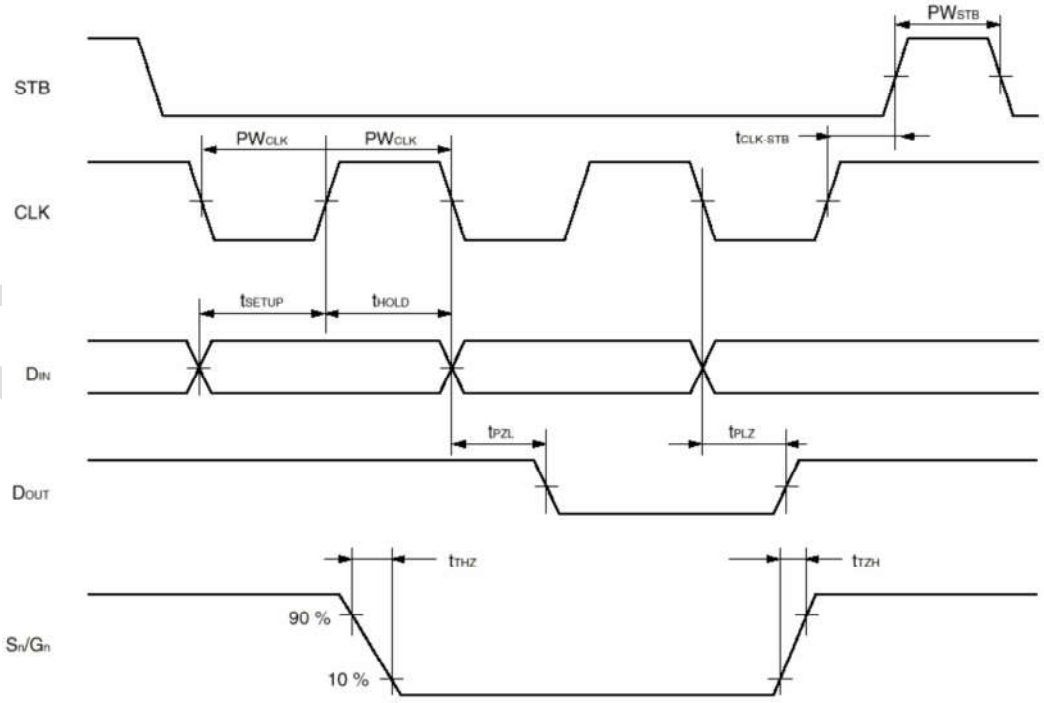
Switching characteristics(VDD = 4.5 ～ 5.5 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test conditions	
Oscillation frequency	fosc	-	500	-	KHz	R = 16.5 KΩ	
Transmission delay time	tPLZ	-	-	300	ns	CLK → DIO	
	tPZL	-	-	100	ns	CL = 15pF, RL = 10K Ω	
Rise time	TTZH 1	-	-	1	μs	CL = 300p F	Seg1～Seg12
Decline time	TTHZ	-	-	1	μs		
Maximum clock frequency	Fmax	1	-	-	MHz	Duty cycle 50%	
Input capacitance	CI	-	-	15	pF	-	

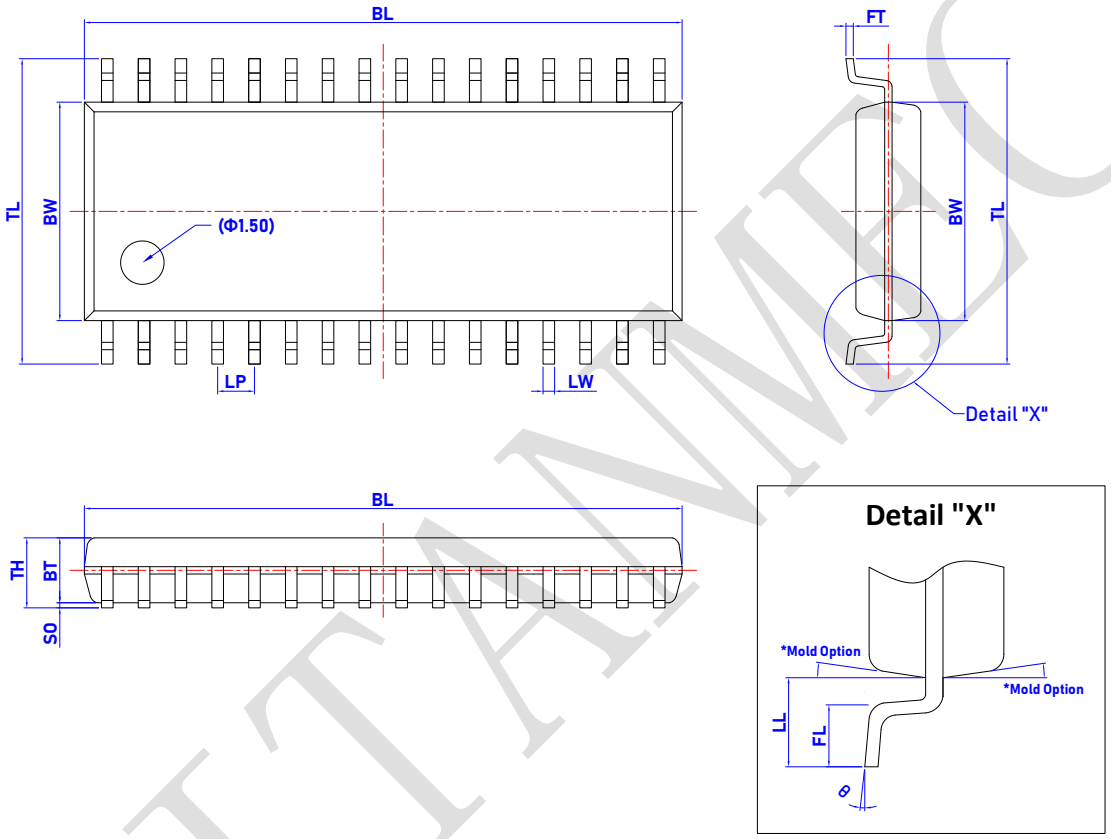
Temporal characteristic(VDD = 4.5 ～ 5.5 V)

Parameter	**Symbol**	Minimum	Typical	Maximum	Unit	Test conditions
Clock pulse width	PWCLK	400	-	-	ns	-
Gate pulse width	PWSTB	1	-	-	μs	-
Data establishment time	tSETUP	100	-	-	ns	-
Data retention time	tHOLD	100	-	-	ns	-
CLK → STB time	tCLK STB	1	-	-	μs	CLK↑→STB↑
Waiting time	tWAIT	1	-	-	μs	CLK↑→CLK↓

Time sequence oscillogram:



XIII. Package size (SOP32-300)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	20.73 (20.63) 20.53	7.64 (7.54) 7.44	10.60 (10.40) 10.20	0.400 TYP	1.270 TYP	0.250 (0.200) 0.170	2.34 (2.24) 2.14	0.250 (0.175) 0.100	2.490 Max.	1.60 (1.50) 1.40	0.95 (0.75) 0.55	8 (4) 0

- All specs and applications shown above subject to change without prior notice.