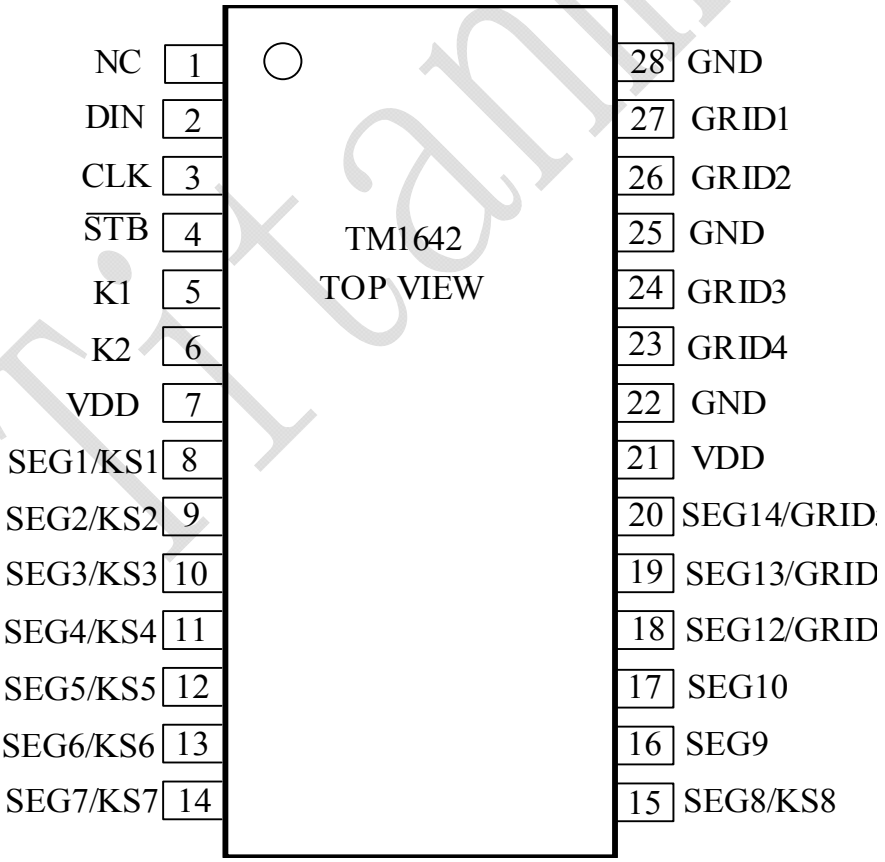
Feature Description

TM1642 is a constant current LED (light emitting diode display) drive control special circuit with the key scan interface, internal integrated with MCU digital interface, data flip-latch, LED high voltage driver, key scan circuit, etc. This product has excellent performance and reliable in quality, mainly applicable for the constant current display driver of segment code LED products. SOP28 encapsulation form is adopted.

Functional Feature

- Adopt power CMOS process
- A variety of display modes (10 segments ×7 bits ～ 13 segments×4 bits)
- SEG constant current drive maximum voltage value: VDD - 1 V
- Channel difference maximum + / - 3%
  Maximum between the chips + / - 6%
- Key scan (8 x 2)
- Luminance adjustment circuit (8-level software adjustable constant current)
- Serial interface (CLK, STB, DIN)
- Oscillation mode: built-in RC oscillator (+ 5%) 450 KHZ
- Built-in electric reset circuit
- Encapsulation form: SOP28

Pin Information

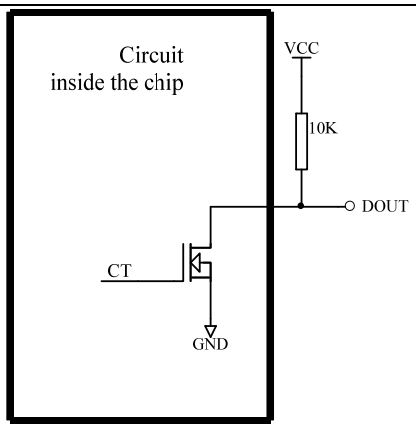


SOP28

Pin Function

Symbol	Pin Name	Pin No.	Description
DIN	Data output Data input	2	On the rising edge of the clock input serial data, starting from the low bit, N tube open drain output, external pull up resistors 10 k is accessed when using the key.
CLK	Clock input	3	On the rising edge read serial data, on the trailing edge output data
STB	CS	4	On the rising or trailing edge initialize serial interface, then wait to receive command. After STB is low the first byte is as the command, when processing the command, the other current processing is terminated. When STB is high, CLK is ignored
NC	NC	1	Not interconnections
K1～K2	Key scan data input	5～6	The input data of the pin at the end of the display cycle with latch
SGE1/KS1～ SEG8/KS8	Output (segment)	8～15	Segment constant flow output (also used as key scan), P tube open drain output
SEG9~SEG10	Output (segment)	16~17	Segment constant flow output, P tube open drain output
GRID1～ GRID4	Output（bit）	27、26 24、23	Bit output, N tube open drain output
SEG12/DRID7 ～ SEG14/GRID5	Output (segment/bit)	18～20	Segment/bit multiplexing output, only segment or bit output selected
VDD	Logic power supply	7、21	System power
GND	Ground	22、25、28	System grounding

▲ **Note**: DIN output data for N tube open drain output, it requires external pull up resistors of 1K-10K while reading the key, as shown in Figure (1). The company recommends pull up resistance of 10K. On the trailing edge of the clock DOUT controls N tube, the reading is not stable, refer to Figure (4), only on the rising edge of the clock the readings are stable.



Circuit inside the chip
Figure (1)

Display Register

External devices transfer data through serial interface to TM1642 display register, from address 00H – 0DH total 14 bytes unit, corresponding to chip SEG and pin GRID connected LED lamp respectively, distribution is shown in Table (1). When writing the LED display data, Display address from low to high, from the low to high data bytes.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	X	X	
xxHL (Low four bit)				xxHU(High four bit)				xxHL(Low four bit)				xxHU (High four bit)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				**GRID1**
02HL				02HU				03HL				03HU				**GRID2**
04HL				04HU				05HL				05HU				**GRID3**
06HL				06HU				07HL				07HU				**GRID4**
08HL				08HU				09HL				09HU				**GRID5**
0AHL				0AHU				0BHL				0BHU				**GRID6**
0CHL				0CHU				0DHL				0DHU				**GRID7**

Table (1)

Key scan and key data register

Key can matrix is 8 x 2 bit, as shown in Figure (2) :

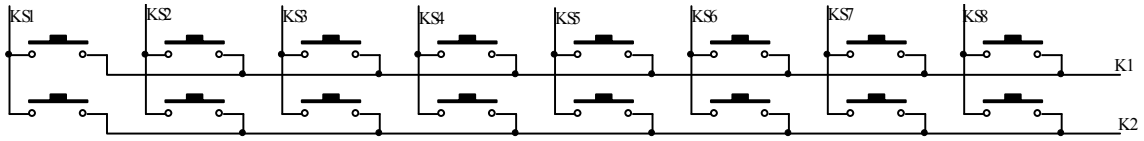


Figure (2)

Key scan data storage address is shown in Table (2). After reading key command is sent, begin to read in turn key data BYTE1—BYTE5 byte, read data from low bit, in which B6 and B7 bit are invalid, and chip output is zero at this time. When chip K and pin KS corresponding key is pressed, the corresponding BIT in the byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K1	K2	X	K1	K2	X			
KS1			KS2			0	0	BYTE1
KS3			KS4			0	0	BYTE2
KS5			KS6			0	0	BYTE3
KS7			KS8			0	0	BYTE4

Table（2）

▲Note:

1. TM1642 can be read maximum 4 bytes, not allowed to read more.
2. Data byte can only be read sequentially from BYTE1 - BYTE4, not allowed to read across the bytes. For example: when hardware K1 and KS8 corresponding keys are pressed, to read this key data at this time, 4 bytes 4 bit is required to be read to read the data; when K1 and KS8 are pressed, read data B3 by BYTE4 is 1 at this time.
3. The combination key can only be the same KS, only different K pin can make key combination; Not the same K with different KS pin can be used as key combination.

Command Description

Command is used to set the display mode and state of LED driver.

On the trailing edge of STB by DIN input the first byte as a command. After decoding, with the highest two bits B7, B6 to differentiate different commands

B7	B6	Command
0	0	Display mode setting command
0	1	Read and write data setting command
1	0	Display control command
1	1	Address setting command

If STB is set to high level upon the command or data transmission, serial communication is initialized, and command or data being sent is invalid (prior command or data transmission remains valid).

(1) Display mode setting command:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display mode
0	0	For outlier, fill in 0				0	0	4 bits 13 segments
0	0					0	1	5 bits 12 segments
0	0					1	0	6 bits 11 segments
0	0					1	1	7 bits 10 segments

This command is used to set the number of the selected segment and bit (4 ~ 7 bits, 10 ~ 13 segments). Upon the command execution, display is forced to shut down, it requires to send display control command to open, and the original display data content will not be changed. But when the same mode is set, the above situation will not occur. Upon access to electricity, the default mode setting is 7 bits 11 segments.

（2）Read and write data setting command:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	For outlier, fill in 0				0	0	Data read and write mode setting	Write data to the display register
0	1					1	0		Read key scan data
0	1				0			Address adding mode setting	Address automatically adding
0	1				1				Fixed address
0	1			0				Test mode setting (internal use)	Normal mode
0	1			1					Test mode

This command is used to set data read and write, B1 and B0 bits are not allowed to set 01 or 11.

(3) Address setting command:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display Address
1	1	For outlier, fill in 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH

This command is used to install display register address.
If the address is set to 0EH or higher, the data is ignored, until the effective address is set.
Upon access to electricity, the address default set is 00H.

(4) Display control command:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	Fill in 0 for outlier			0	0	0	Display brightness setting	Set constant flow ratio as 1/16
1	0				0	0	1		Set constant flow ratio as 2/16
1	0				0	1	0		Set constant flow ratio as 4/16
1	0				0	1	1		Set constant flow ratio as 10/16
1	0				1	0	0		Set constant flow ratio as 11/16
1	0				1	0	1		Set constant flow ratio as 12/16
1	0				1	1	0		Set constant flow ratio as 13/16
1	0				1	1	1		Set constant flow ratio as 14/16
1	0			0				Display switch setting	Display off
1	0			1					Display on

Serial data transmission formats

Read and accept 1 BIT operation on the rising edge of clock.

Data reception (write data)

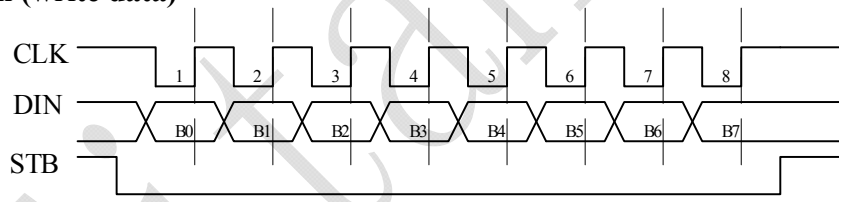


Figure (3)

Data reading (read data)

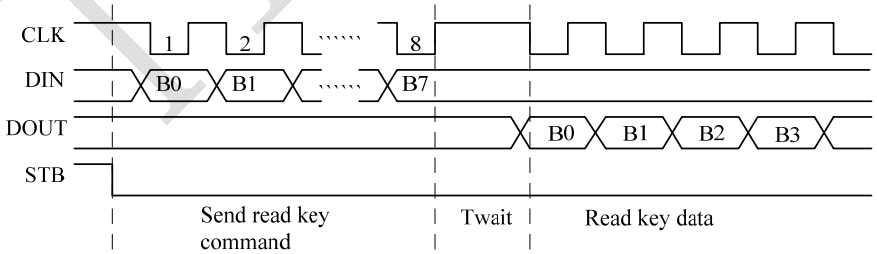


Figure (4)

▲**Note**: While reading data, from the serial clock CLK eighth rising edge start setting commands to the CLK falling edge data reading it requires the waiting time Twait (minimum 1μS).

Display and keys

(1) **Display**:

1. Drive common cathode digital tube:

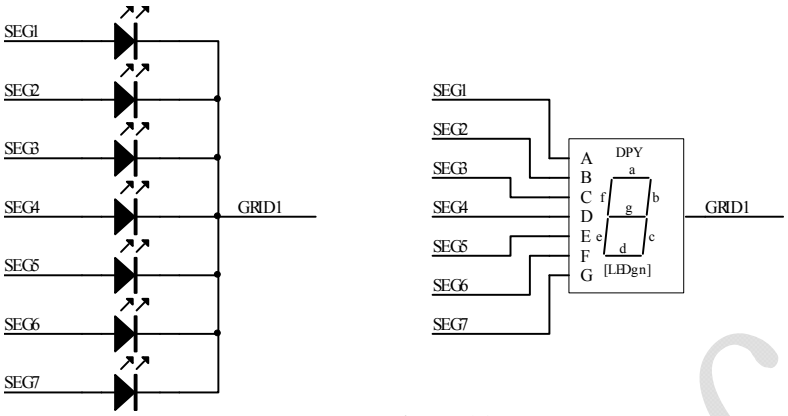


Figure (5)

Figure (5) shows the common cathode digital tube connection diagram, if let the digital tube display "0", then it is required to let the SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 as high level and SEG7 as low level when GRID1 is low level, refer to Table (1) the address display form, simply by reading data 3FH in the address 00H to let the digital tube display "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

2. Drive common anode digital tube:

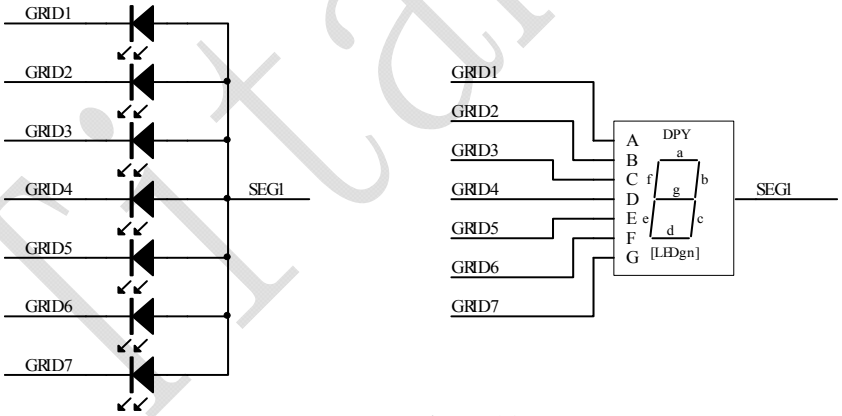


Figure (6)

Figure (6) shows the common anode digital tube connection diagram, if let the digital tube display "0", then it is required to let the SEG1 as high level when GRID1, GRID2, GRID3, GRID4, GRID5, GRID6 are low level, and let SEG1 as low level when GRID7 is low level. It is required to write data 00H to address unit 00H, 02H, 04H, 06H, 08H, 0AH respectively.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0AH
0	0	0	0	0	0	0	0	0CH
B7	B6	B5	B4	B3	B2	B1	B0	

▲**Note**：SEG1-11 is P tube open drain output, GRID1-7 is N tube open drain output, when using, SEG1 11 can only be connected to LED anode, and GRID can only be connected to LED cathode, reverse not allowed.

（2）**Keys:**

Key scan is automatically completed by TM1642, not controlled by the user, the user only need to read the key values in accordance with the temporal sequence. To complete a key scan it takestwo display cycles, one display cycle requires approximately T = 8×500us, at MS press 2 different output keys, two key values readings are the key value of the first pressed key.

Display Figure (7) use the oscilloscope to observen SEG1 / KS1 and SEG2 / KS2 output key scan waveform, as shown in Figure (8).

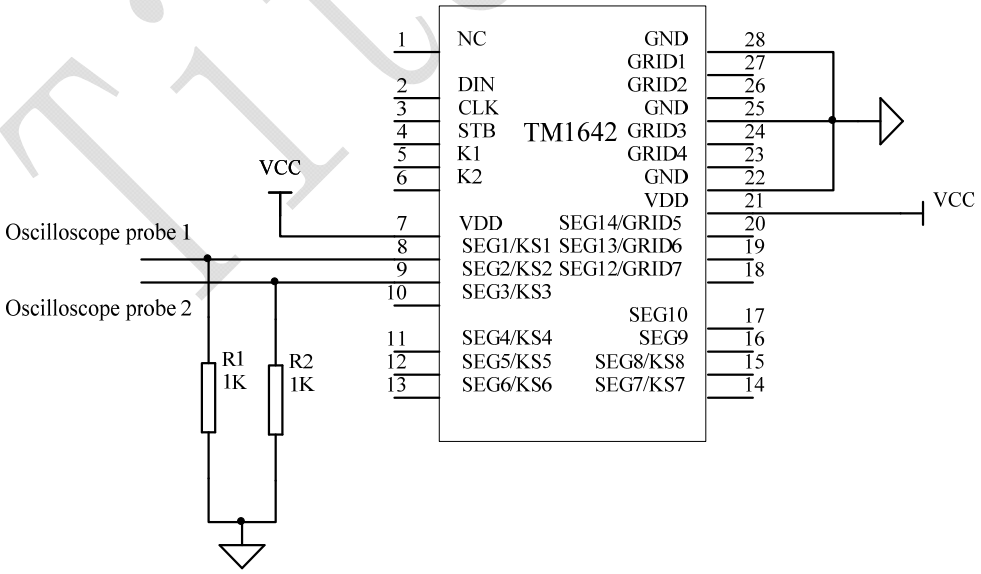


Figure (7)

During the IC key scan the SEGn/KSn waveform:

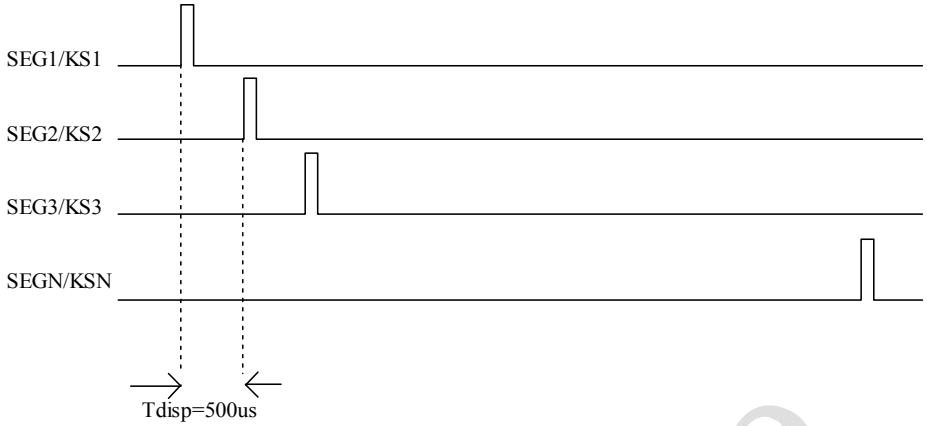


Figure (8)

Tdisp is related to the working oscillation frequency of IC, 500us are for reference only, the actual measurement shall prevail.

In general, use Figure (9), which can meet the requirements of the key design.

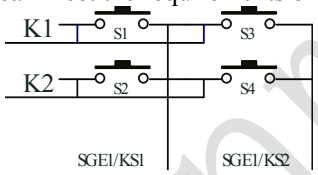
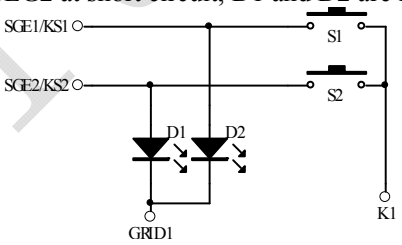


Figure (9)

When S1 is pressed, at the first byte B0 reads "1". If more than one key are pressed, it will read multiple "1"s, when S2, S3 are pressed, it can read "1" at B1, B3 of the first byte.

▲**Note**: Combination key use notice:

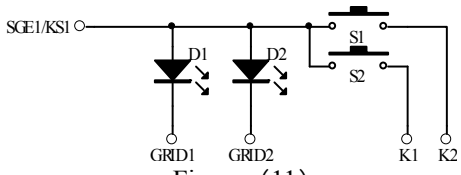
SEG1 / KS1 - SEG10 / KS10 is display and key scan combination use. Take Figure (10) as an example, the display requires to let D1 light, D2 off, and let SEG1 as "1", SEG2 as "0" state, if S1, S2 are pressed at the same time, it is equivalent to SEG1, SEG2 at short circuit, D1 and D2 are lit up at this time.



Figure（10）

Solutions:

1. On the hardware, it can set the required keys to be pressed at the same time on different K line as shown in Figure (11):



Figure（11）

2. Series resistance on the SEG1 - SEG N as shown in Figure (12), the resistance value shall be selected at 510 ohm, too much resistance will cause the failure of keys, too little resistance may not be able to solve the problem of display interference.

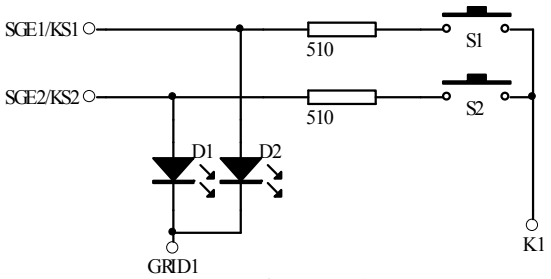


Figure (12)

3. Or series diode as shown in Figure (13) :

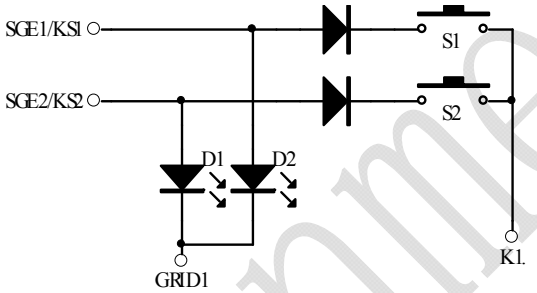
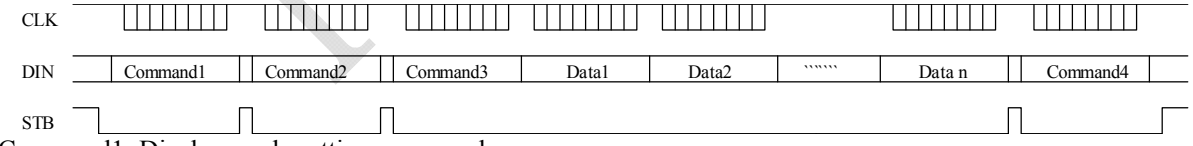


Figure (13)

In application serial data transmission

(1) Address automatic plus one mode

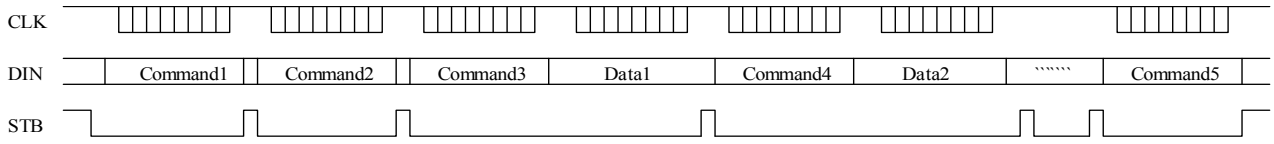
Use address automatic plus 1 mode, setting the address is actually setting the starting address of the data flow storage. Starting address command word is sent, "STB" is not required to be set high followed by the data transmission, up to 14BYTE, only after the data is transmitted set "STB" high.



Command1: Display mode setting command
Command2: Read and write data setting command
Command3: Display address setting command
Data1 ~ n: Display data, with Command3 specified address as the starting address (up to 14 bytes)
Command4: Display control command

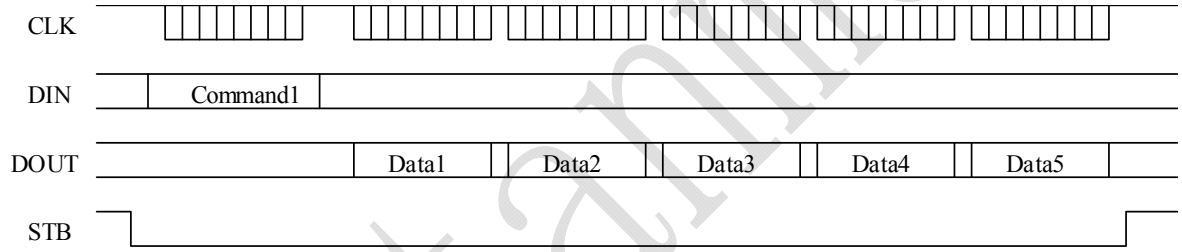
（2） Fixed address mode

Using a fixed address mode, setting the address is actually setting the required 1 byte data storage address. After the address is sent, "STB" is not required to set high, followed by 1 byte data transmission, only after the data is transmitted set "STB" high. And then reset the address required for the storage of the second data, up to 14 bytes data is transmitted, and set "STB" high.



Command1: Display mode setting command
Command2: Read and write data setting command
Command3: Display address setting command, set display address as 1
Data1: Display data 1, store in the Command3 specified address unit
Command4: Display address setting command, set display address as 2
Data2: Display data 2, store into Command4 specified address unit
Command5: Display control command

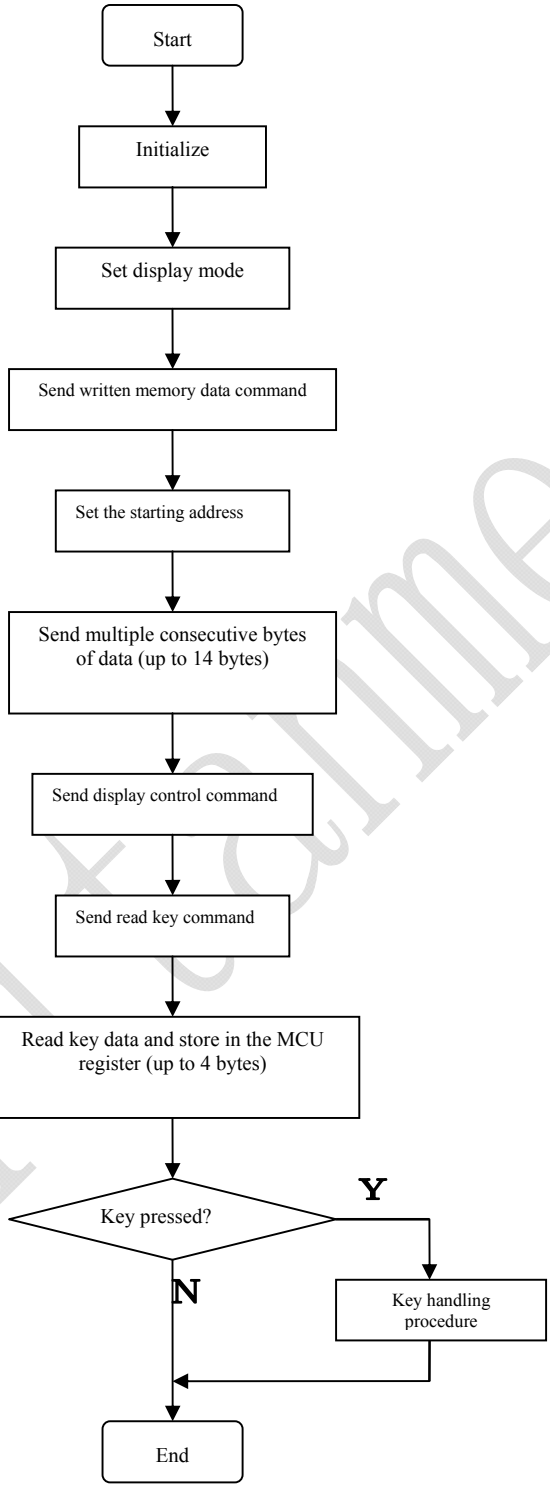
(3) Read key sequence



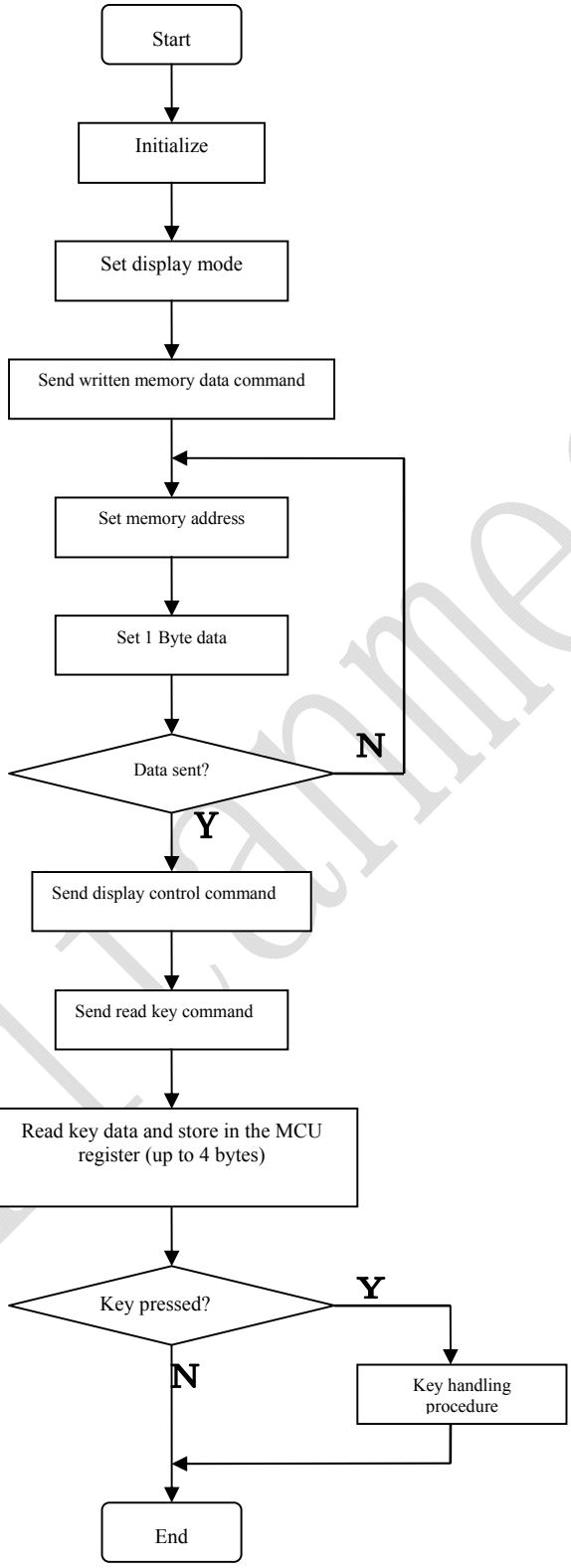
Command1: Read key command
Data1 ~ 5: Read the key data

(4) Programming

Using address automatic plus one mode program flow chart:



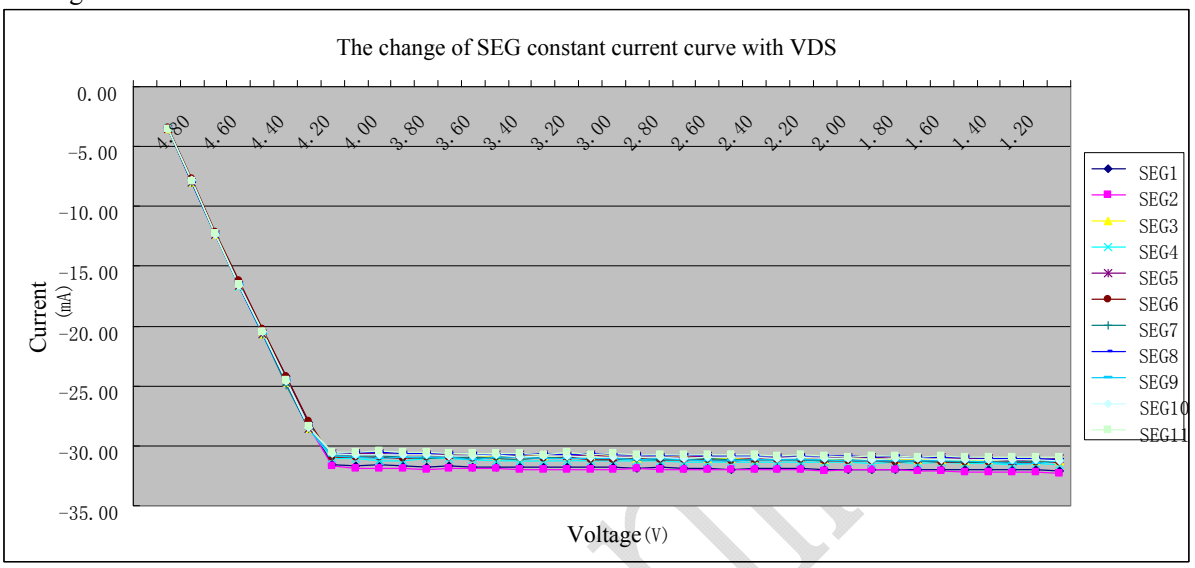
Figure：Adopt the fixed address program design flow chart:



Constant current control circuit

TM1642 supports constant current drive application, to apply in high-end applications of display driver.

1. The maximum current error between channels is less than ±3%, while the maximum current error between chips is less than ±6%.
2. At the constant current linear area working, it shall ensure the SEG pin and GND differential pressure to be less than 4V.
3. In addition, when the VDS changes, the stability of the output current is not affected, as shown in the Figure below



Encapsulation heat dissipating power (PD)

Encapsulation maximum heat dissipating power is determined by the formula:

$$P_{D(max)}=\frac{(T_j-T_a)}{R_{th(j-a)}}$$

When 11 channels are completely opened, the actual power consumption is:

$PD(act)=I_{DD}*V_{DD}+I_{OUT}*Duty*V_{DS}*11$

The actual power consumption must be smaller than the maximum power consumption, namely $PD(act)<PD(max)$, in order to keep $PD(act)<PD(max)$, the relationship between the maximum current and constant current output is as follows:

$$I_{OUT}=\frac{[\frac{(T_j-T_a)}{R_{th(j-a)}}-I_{DD}*V_{DD}]}{V_{DS}*Duty*11}$$

In which Tj is the working temperature of IC, Ta is the ambient temperature, V_{DS} is the steady flow output port voltage, Duty is the constant current ratio 14/16, Rth(j - a) is the encapsulation of thermal resistance.

Application circuit

TM1642 drive common cathode digital panel wiring circuit:

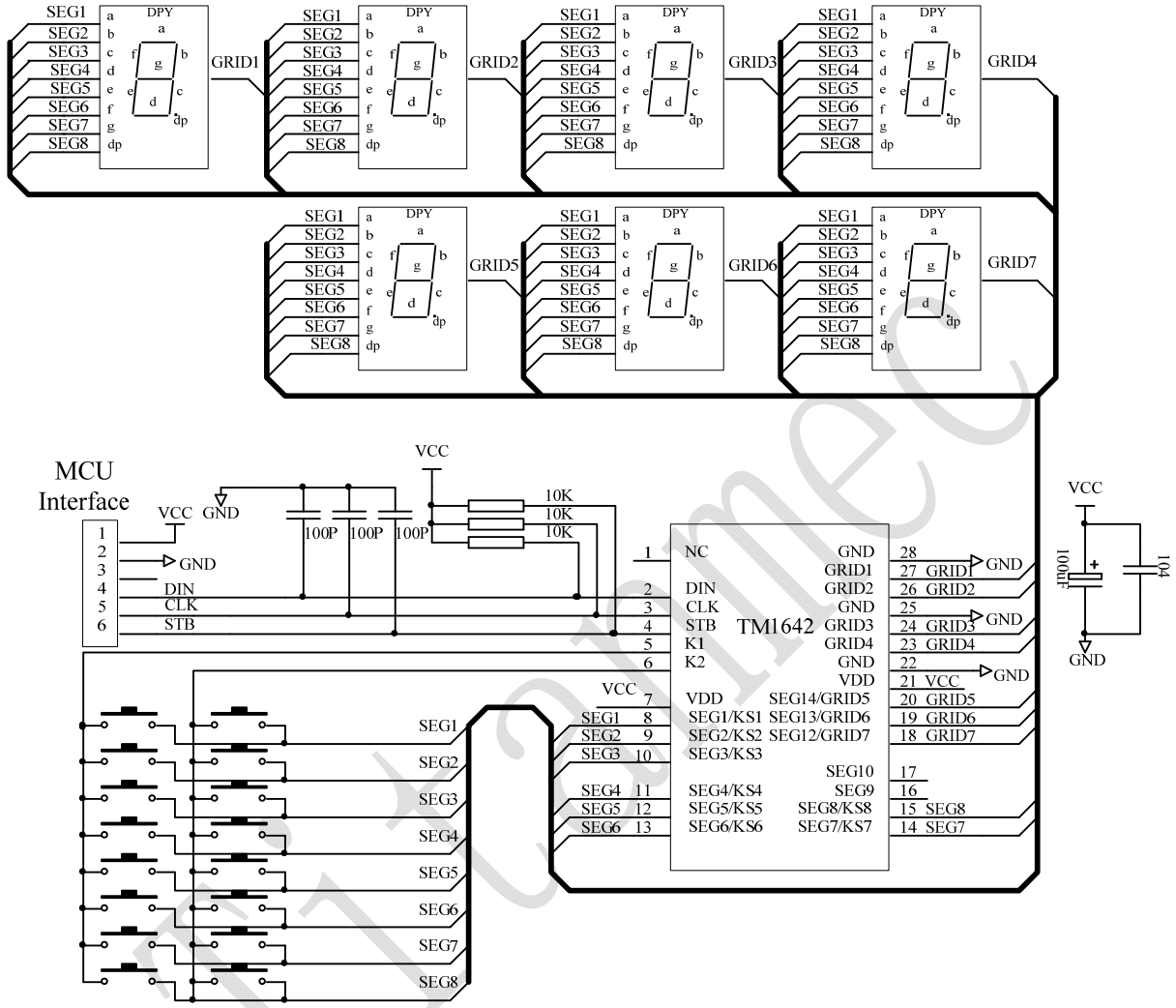


Figure (14)

▲Note:

1. Between VDD and GND the filter capacitance wiring at PCB should be placed as close to the TM1642 chip as possible, so as to strengthen the filtering effect.
2. The three 100P capacitance connected to DIN, CLK, STB communication port can reduce the disturbance to the communication port.
3. As blu-ray digital tube conduction pressure drop is about 3V, select 5V power supply for TM1642.
4. In order to make the chip into constant current linear work area, please make sure the SEG channel and GND pressure drop is less than 4V.

TM1642 drive common anode digital panel wiring circuit:

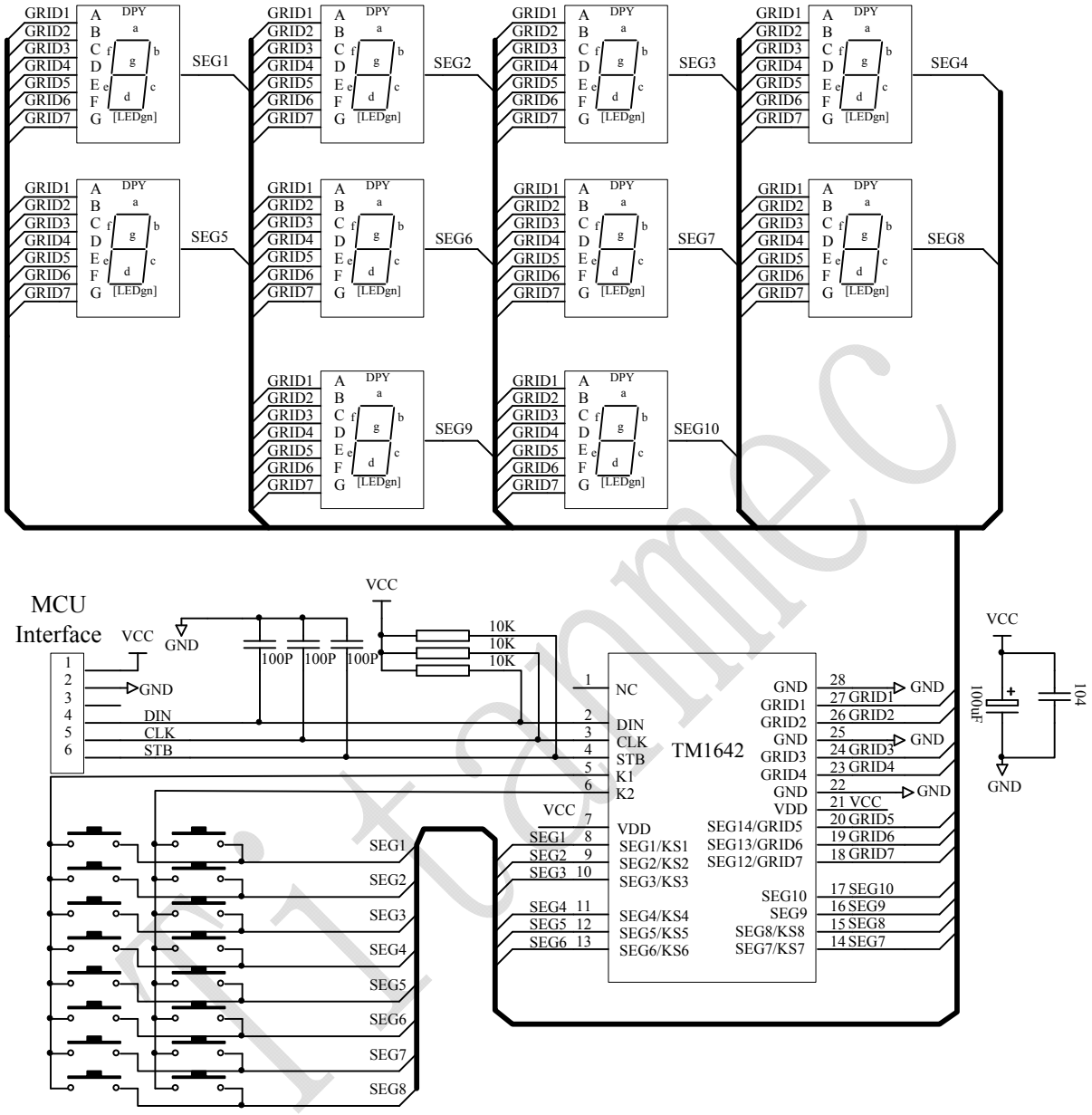


Figure (15)

▲Note:

1. Between VDD and GND the filter capacitance wiring at PCB should be placed as close to the TM1642 chip as possible, so as to strengthen the filtering effect.

2. The three 100P capacitance connected to DIN, CLK, STB communication port can reduce the disturbance to the communication port.

3. As blu-ray digital tube conduction pressure drop is about 3V, select 5V power supply for TM1642.

4. In order to make the chip into constant current linear work area, please make sure the SEG channel and GND pressure drop is less than 4V.

Electrical Parameters

Limit Parameters (Ta = 25 ℃, Vss = 0 V)

Parameter	Symbol	Range	Unit
Logic power supply voltage	VDD	-0.5 ～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
SEG LED driver output current	IO1	-40	mA
LED GRID driver output current	IO2	+200	mA
Power loss	PD	400	mW
Working temperature	Topt	-40 ～ +80	℃
Storage temperature	Tstg	-65 ～+150	℃

Normal working range（Ta = -20 ～ +70℃，Vss = 0 V）

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
Logic power supply voltage	VDD	4	5	7	V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

Electrical characteristics（Ta = -20 ～ +70℃，VDD = 4.5 ～ 5.5 V， Vss = 0 V

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
High level constant current output current	Ioh1	28	35	40	mA	Seg1~Seg11， Vo = vdd-2V Constant current ratio 14/16
	Ioh2	28	35	40	mA	Seg1~Seg11， Vo = vdd-3V Constant current ratio 14/16
Low level input current	IOL1	80	140	-	mA	Grid1~Grid6 Vo=0.4V
Low level output current	Idout	4	-	-	mA	VO = 0.4V，dout
High level output current tolerance	Itolsg	-	-	5	%	VO = VDD – 3V， Seg1～Seg11
Output pull down resistor	RL		10		KΩ	K1~K3

Input current	II	-	-	±1	μA	VI = VDD / VSS
High level input voltage	VIH	0.7 VDD	-		V	CLK，DIN，STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK，DIN，STB
Hysteresis voltage	VH	-	0.35	-	V	CLK，DIN，STB
Dynamic current loss	IDDdyn	-	-	5	mA	No load, display off

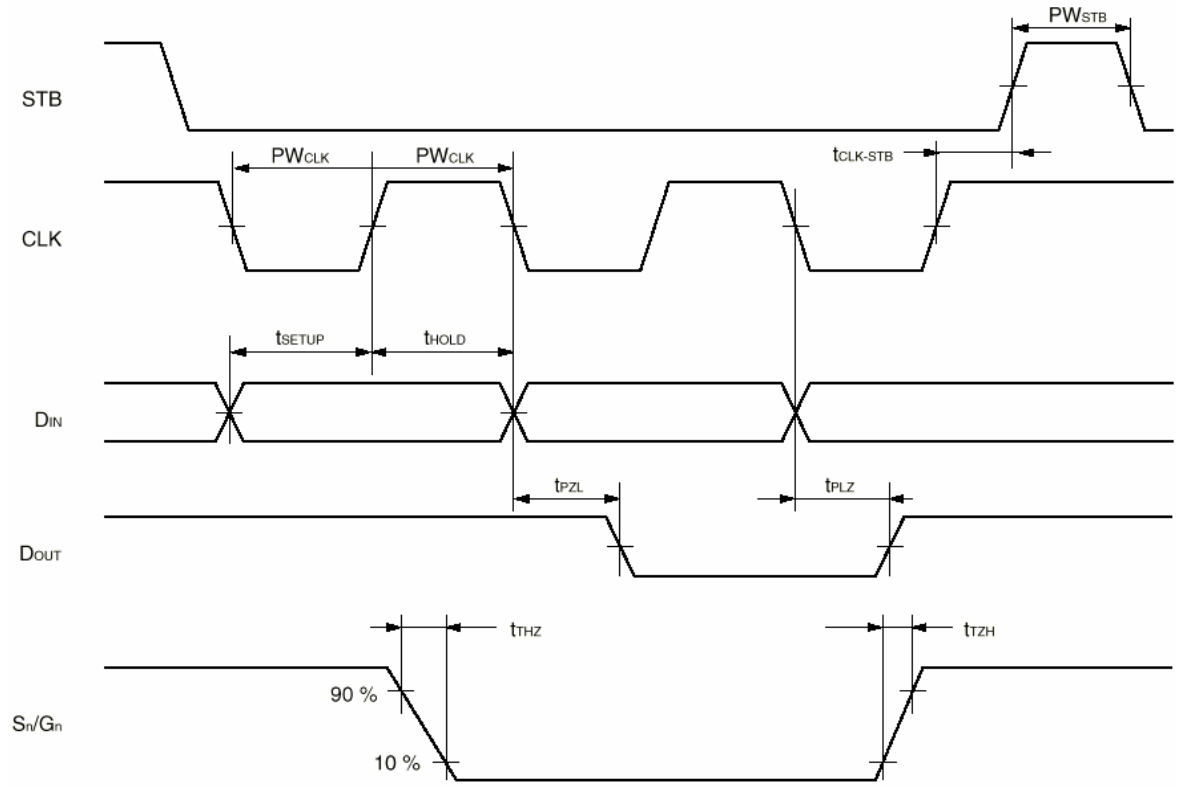
Switch characteristics（Ta = -20 ～ +70℃，VDD = 4.5 ～ 5.5 V）

Parameter	Symbol	Min	Typical	Max	Unit	Test condition	
Oscillation frequency	fosc	-	500	-	KHz	R = 16.5 KΩ	
Transmission delay time	tPLZ	-	-	300	ns	CLK → DOUT	
	tPZL	-	-	100	ns	CL = 15pF, RL = 10K Ω	
Rise time	TTZH 1	-	-	2	μs	CL = 300p F	SEG1～SEG11
	TTZH 2	-	-	0.5	μs		Grid1～Grid4 SEG12/Grid7～SEG14/Grid5
Fall time	TTHZ	-	-	120	μs	CL = 300pF，Segn， Gridn	
Maximum clock frequency	Fmax	1	-	-	MHz	% Duty ratio 50	
Input capacitance	CI	-	-	15	pF	-	

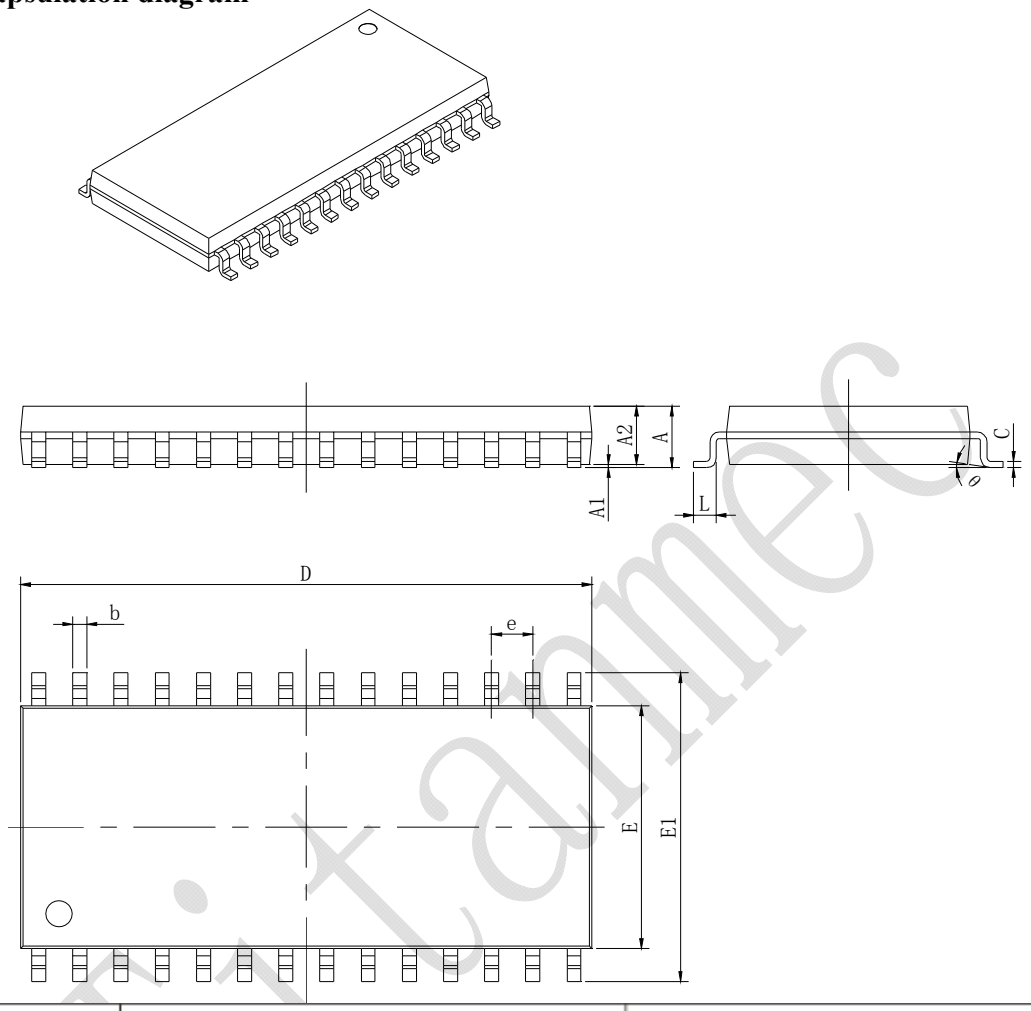
Temporal characteristics（Ta = -20 ～ +70℃，VDD = 4.5 ～ 5.5 V）

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
Clock pulse width	PWCLK	400	-	-	ns	-
Gating pulse width	PWSTB	1	-	-	μs	-
Data setup time	tSETUP	100	-	-	ns	-
Data retention time	tHOLD	100	-	-	ns	-
CLK →STB time	tCLK STB	1	-	-	μs	CLK↑→STB↑
Waiting time	tWAIT	1	-	-	μs	CLK↑→CLK↓

Temporal waveform diagram



Encapsulation diagram



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.290	2.500	0.09	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	17.700	18.100	0.697	0.713
E	7.400	7.700	0.291	0.303
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

- All specs and applications shown above are subject to change without prior notice.