Overview

TM1652 is a dedicated chip for LED (light-emitting diode, digital tube, lattice screen) driver control. It integrates with digital communication circuit, decoding circuit, data latch, oscillator and LED driver circuit. The communication mode adopts UART protocol, hence the chip only receives the data sent from a MCU. Only one TX port of the MCU is required to send data to the chip to achieve single-wire communication. In terms of display driver, the chip adopts dynamic scanning, with two optional display modes, 8-level adjustable segment drive current and 16-level adjustable duty ratio. Besides, TM1652 has built-in blanking circuit which has been optimized.

The product is widely applied in various consuming electronic products, such as air conditioner panel, washing machine panel, DVD display panel and STB display. It boasts excellent performance and reliable quality.

Features

- Low power consumption CMOS workmanship
- Typical operating voltage: 5V
- Common-cathode digital tube display supported
- Two display modes (7 segments × 6grids, 8 segments × 5 grids)
- Luminance adjustment circuit (16-level adjustable duty ratio, 8-level adjustable segment drive current)
- Serial port (SDA), compatible with serial port communication (UART) protocol, baud rate 19200bps supported
- Built-in OSC frequency 2.5M
- Built-in power-on reset circuit
- Built-in optimized circuit aiming at brightness
- Packaging mode: SOP16、TSSOP16

Block diagram for internal structure

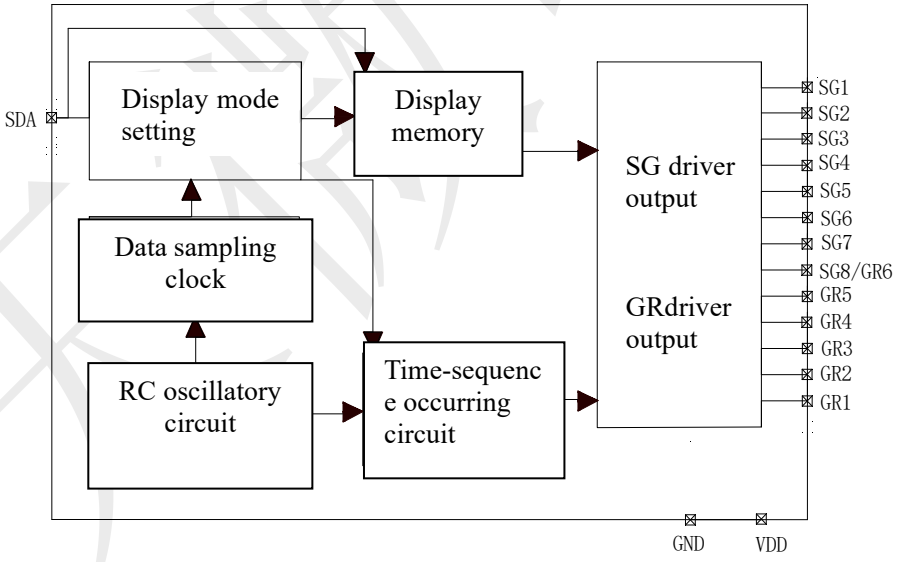


Figure 1

Pin configuration

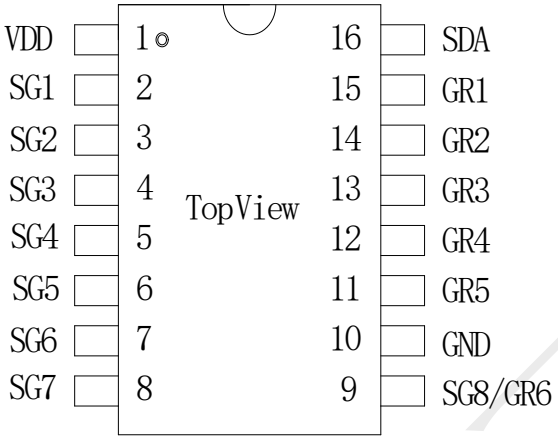


Figure 2

Pin function

Pin name	Pin number	I/O	Function description
VDD	1	--	Positive power supply
SG1～SG7	2～8	O	Segment output, built-in PMOS, 8-level adjustable drive current, used to drive LED source current output
SG8/GR6	9	O	Segment/Gridmultiplexing output, for both SEG and GRID functions, configured by software
GR1～GR5	11～15	O	Grid output, built-in NMOS, 16-level adjustable duty ratio, used to drive LED sink current output
GND	10	--	Power ground
SDA	16	I	Data input pin

Note: SG8/GR6 multiplexing output pin cannot be simultaneously connected onto the segment drive pin and grid driving pin of the digital tube. If so, it will cause digital brightness mistake and lead to abnormal display.

Input and output equivalent circuit

Figure 3

Integrated circuit is an electrostatic sensitive device which tends to generate a lot of static electricity when used in a dry season or dry environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics suggests taking all appropriate preventive measures for integrated circuit. Improper operation and welding might cause ESD damage or performance reduction and chip operation failure.

Limit parameters

Parameter name	Parameter symbol	Limit value	Unit
Logic supply voltage	VDD	+7.0	V
Logic input voltage	VI1	VDD + 0.5	V
GR drive output current	IO2	170mA@0.3V	mA
Power loss	PD	400	mW
Operating temperature	Topt	-40 ～ +80	℃
Storage temperature	Tstg	-65 ～+150	℃
ESD	Human body model (HBM)	3000	V
	Machine model (MM)	200	V

(1) When the chip works for a long time under the above limit parameters, it may cause device reliability reduction or permanent damage. Titan Micro Electronics does not suggest any parameter reaching or exceeding the limit value in practical use.
(2) All voltage values are comparatively tested in a systematic ground.

Recommended operating conditions

Tested under -45℃-+85℃, unless otherwise specified			TM1652			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Logic supply voltage	VDD	—	3	5	6	V
High level input voltage	VIH	—	0.7VDD	—	VDD	V
Low level input voltage	VIL	—	0	—	0.3VDD	V

Electrical characteristics

Tested under -20℃-+85℃, unless otherwise specified; VDD = 5 V, GND = 0 V			TM1652			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
SG high level output current	Ioh1	SG driving strength 8/8, SG1-SG8 ports resort to 3V applied voltage test at high level	20	25	30	mA
	Ioh2	SG driving strength 8/8, SG1-SG8 ports resort to 2V applied voltage test at high level	20	30	40	mA
GR low level input current	IOL1	SG1-SG6 ports resort to 0.3V applied voltage test at low level	80	140	—	mA
SDA input current	Isda	VDD = 5V, other pins are suspended.	—	—	±1	μA
High level input voltage	VIH	VDD=5V	0.7 VDD	—	—	V
Low level input voltage	VIL	VDD=5V	—	—	0.3 VDD	V
Lagging voltage	VH	VDD=5V	—	0.35	—	V
Dynamic current loss	IDDdyn	No load and display off	—	—	5	mA

Switch characteristics

Tested under -20℃-+85℃, unless otherwise specified; VDD = 5 V, GND = 0 V			TM1652			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Internal oscillation frequency	fosc	—	—	2.5	—	MHz
GR scanning cycle	Fgr	SG8*GR5 mode	450	500	550	Hz
		SG7*GR6 mode	370	420	470	
Baud rate bit width range	Bsda	VDD = 5V	47	52	57	μs
SDA data frequency	Fmax	Duty ratio 50%	1	—	—	MHz
SDA input capacitor	CI	—	—	—	15	pF

Function description

1. Communication protocol

The chip adopts UART protocol. Its operating principle is transmitting the characters of transmitted data one bit after the other bit in serial mode. The following figure shows this operating principle:

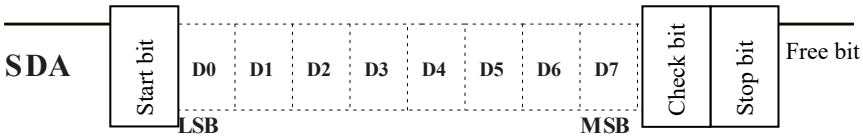


Figure 4

The time for each bit of TM165 is: 52us.

The meaning of each bit is as follows:

▲Start bit: from high to low, low level time being the time of one bit, representing the start of transmitted characters.

▲Data bit: right after start bit, D0-D7, with lower bit sent first.

▲Check bit: the time of one bit, if the number of 1 in 8 data bits is odd, this bit is set as 0 (set with low level), or else it is set as 1 (set with high level).

▲Stop bit: set to high position, the time of one bit, indicating the end of sending one character of data.

▲Free bit: set to high position, if the time for setting free bit to high position is more than 3ms, TM1652 will consider the end of data frame of this time and the data of this time will be entered into corresponding register from temporary storage to start control chip output. If the transmission of a frame of data does not end, it is suggested to set the time of free bit within 0-0.5ms.

A frame of data of TM1652 contains the following two forms:

(1) Display address command + display data;

(2) Display control command + display control adjustment command.

Baud rate: the pointer to measure data transfer rate, representing the number of binary bits transmitted every second. For instance, if data transfer rate is 120 characters/s and each character contains 11 bits, the baud rate of transmission will be 11 × 120 = 1320 bits/s = 1320 bauds. TM1652 supports the baud rate range of 17500bps-21200bps. We suggest using 19200bps, i.e., the time for each bit is: 1s/19200 ≈ 52us. Therefore, the time range for each bit TM1652 supports is: 47us-57us. When IO is used to simulate UART communication, the bit width of SDA data should meet the provided bit width range.

Here we take the baud rate of 19200bps for example. When display control command “0X18” is sent to SDA pin, the time sequence waveform is as follows:

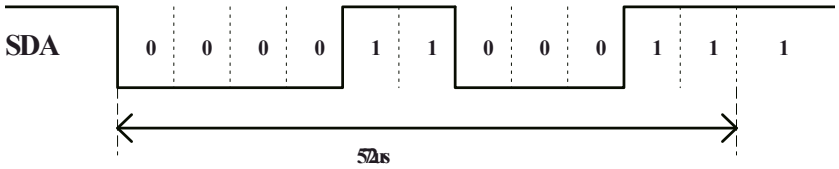


Figure 5

As shown in Figure 5, the "0X18" command sent totally contains 11 bits, which, from left to right, respectively are 1 start bit, 8 data bits, 1 check bit and 1 stop bit. The time for each bit is about 52us and the total time for the 11 bits is about 572us. The binary reading according to the above figure is "00011000", which, when converted to a hexadecimal string, is "0X18".

Note: TM1652 not only receives the control signal sent out by 5V MCU but also receives that by 3.3V MCU. However, it is not suggested to use the systems of different power supplies.

2. Display command description

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Description
Address bit			0	1	0	0	0	Display address command
0	0	0	1					Display control command

B3-B0 are 1000 which are fixed data used for internal clock correction.

3. Display data description

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1

Corresponding to BIT position, setting as "0" means invalid and low level output; setting as "1" means valid and high level output. For example, "0x01" means high SG1 output.

4. Display address command description

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	1	0	0	0	GR1 address
1	0	0						GR2 address
0	1	0						GR3 address
1	1	0						GR4 address
0	0	1						GR5 address
1	0	1						GR6 address

B3-B0 are 1000 which are fixed data used for internal clock correction. When B4 is set as "0", it means the current data are display address commands.

5. Display control adjustment command description

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	0	0	0					Display switch setting	Screen off
1	0	0	0					Grid drive duty ratio setting	Duty ratio set as 1/16
0	1	0	0						Duty ratio set as 2/16
1	1	0	0						Duty ratio set as 3/16
0	0	1	0						Duty ratio set as 4/16
1	0	1	0						Duty ratio set as 5/16
0	1	1	0						Duty ratio set as 6/16
1	1	1	0						Duty ratio set as 7/16
0	0	0	1						Duty ratio set as 8/16
1	0	0	1						Duty ratio set as 9/16
0	1	0	1						Duty ratio set as 10/16
1	1	0	1						Duty ratio set as 11/16
0	0	1	1						Duty ratio set as 12/16
1	0	1	1						Duty ratio set as 13/16
0	1	1	1						Duty ratio set as 14/16
1	1	1	1						Duty ratio set as 15/16
				0	0	0		Segment drive current setting	Segment drive current set as 1/8
				1	0	0			Segment drive current set as 2/8
				0	1	0			Segment drive current set as 3/8
				1	1	0			Segment drive current set as 4/8
				0	0	1			Segment drive current set as 5/8
				1	0	1			Segment drive current set as 6/8
				0	1	1			Segment drive current set as 7/8
				1	1	1			Segment drive current set as 8/8
							0	Display mode setting	Setting output of 8 segments and 5 grids
							1		Setting output of 7 segments and 6 grids

This command is used to set gird duty ratio, segment drive current and display mode selection.

Note: Since the current provided by the chip is not enough to lighten common digital tube when segment drive current is 1/8, it is suggested to at least set segment drive current as 2/8.

Application information

1. Command data definition of TM1652

The first byte is for control command setting, with lower bit sent first. The four lower bits from B3 to B0 are 1,000 which are fixed data. B4 is for register type selection, to select display control command when it is “1” and to select display address command when it is “0”. B7-B5 are for display address setting.

It is data from the second byte, which is sent into the corresponding temporary storage from the address in the first byte. If it is a display control command, the second byte must be the display control adjustment command.

If it is a display address command, it can be multi-byte data, and the subsequent byte data can be placed into the corresponding temporary storage as address +1. If the address exceeds the corresponding valid address and the display address is over 101, the exceeding data is invalid. If the address contained in the first byte exceeds the corresponding valid address or is an invalid address, the data of this time is invalid. Prior to application, it is suggested to send display data first and then control data (display on). If control data is sent first (display on) and display register is not reset, the random data in the display register will be outputted, which leads to garbage code display of digital tube till the display register receives correct display data.

2. Driving common-cathode digital tube

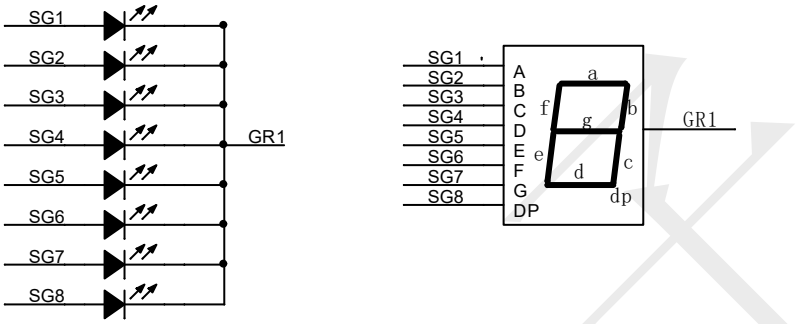


Figure 5

The above figure shows the connection diagram of common-cathode digital tube. If the digital tube displays "0", it needs to set SG1, SG2, SG3, SG4, SG5 and SG6 to high level and set SG7 and SG8 to low level when GR1 is at low level. View the following figure for display address table. To enable the digital tube display "0", it only needs to write data 3FH at 00H display address unit. The detailed data packet is: first send address command "0X08", and then send display data "0X3F", i.e., store "0X3F" into address 00H and output it via SG pin; send "0X00" for other addresses to make the digital tube display nothing, and then set SDA pin to high position for at least 3ms and send display control command and display control adjustment command; when the sending completes, set SDA pin to high position for at least 3ms and the digital tube will display "0".

SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

3. Data packet transmission mode

3.1 Address auto +1 mode

In the address auto +1 mode, to set an address actually means to set the initial address stored in the transferred data flow. When the initial address command is completely sent, send the data (6 bytes at most) immediately, and set data line to high position when data sending completes.

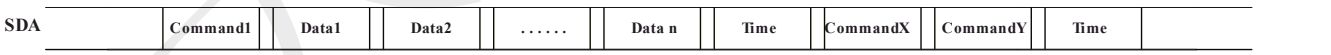


Figure 6

Command1: to select display address command (0x08**)**
Data1-Data n: to send display data (6 bytes at most)
Time: the time for setting data line to high position (the minimum time is 3ms)
CommandX: to select display control command (0x18)
CommandY: to send display control adjustment command (including grid duty ratio, segment drive current and display mode setting)

3.2 Fixed address mode

In the fixed address mode, to set the address actually means to set the address stored in the to-be-transferred 1BYTE display data. When the address is sent completely, send the 1BYTE display data immediately. When data sending completes, set data line to high position for at least 3ms and then send the address, followed by sending the 1BYTE display data and setting data line for at least 3ms to high position again…the rest can be done in the same manner until address and data sending completes.

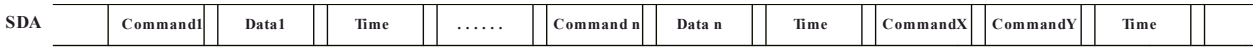


Figure 7

Command1-ommand n: to send display address command, address 1-n (6 addresses can be set at most)
Data1-Data n: to send display data (6 bytes at most)
Time: the time for setting data line to high position (the minimum time is 3ms)
CommandX: to select display control command (0x18)
CommandY: to send display control adjustment command (including grid duty ratio, segment drive current and display mode setting)

The chip does not need a command to set it works in address auto +1 mode or fixed address mode. Strictly speaking, it only has an address auto +1 mode. The division here is to better explain that the chip can separately write display data for a certain display register address. If it is to separately write display data for a certain display address, only one display data can be written right after writing the display address and the signal line needs to be set to high position for at least 3ms; if it is to write several display data right after writing the display address, after the chip receives the first data, the display address will automatically add 1 at specified address and then receive the second display data until the display data of the last display address is received.

4. 7-segment × 6-grid application circuit connection:

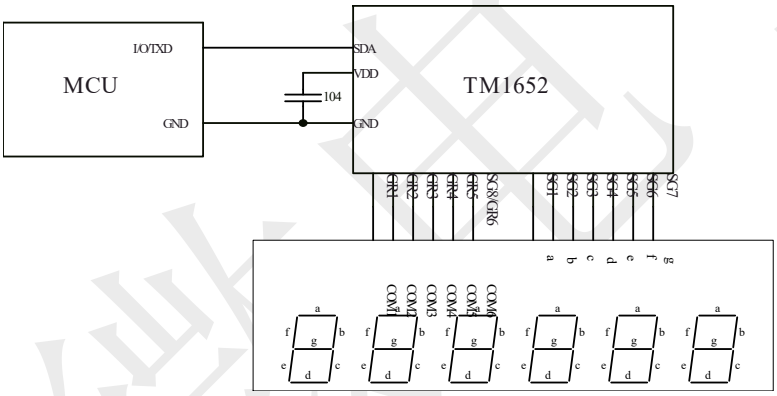


Figure 8

5. 8-segment × 5-grid application circuit connection:

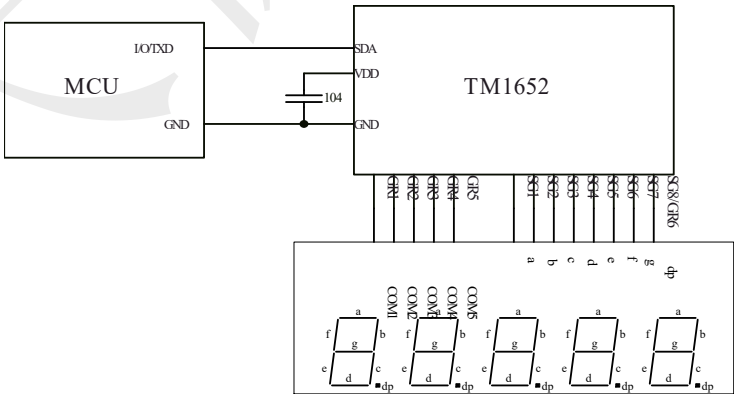
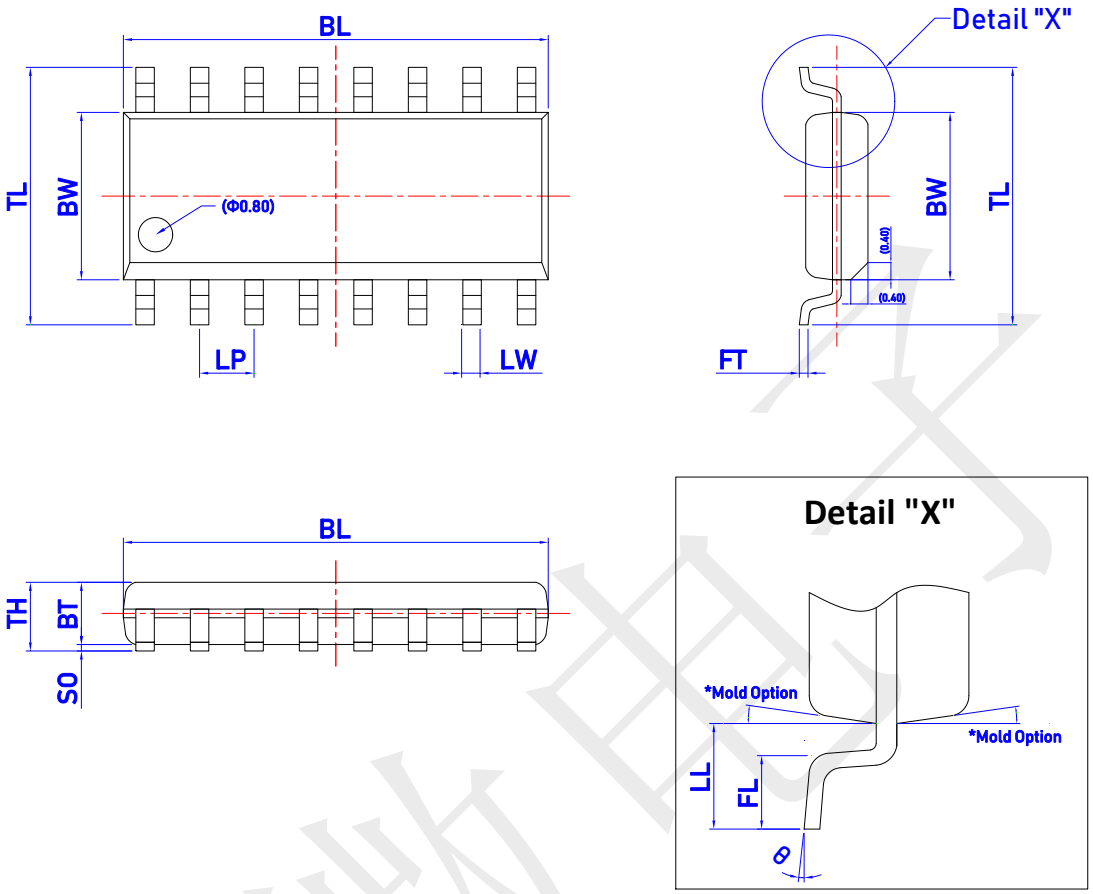


Figure 9

Note: Prior to application, please add a 104 decoupling capacitor on chip VDD and GND. The shorter the connecting line between chip VDD and GND, the better the decoupling effect and the more reliable operation of the chip.
The chip is designed for common-cathode digital tube drivers. It does not apply to common-anode digital tube drivers.

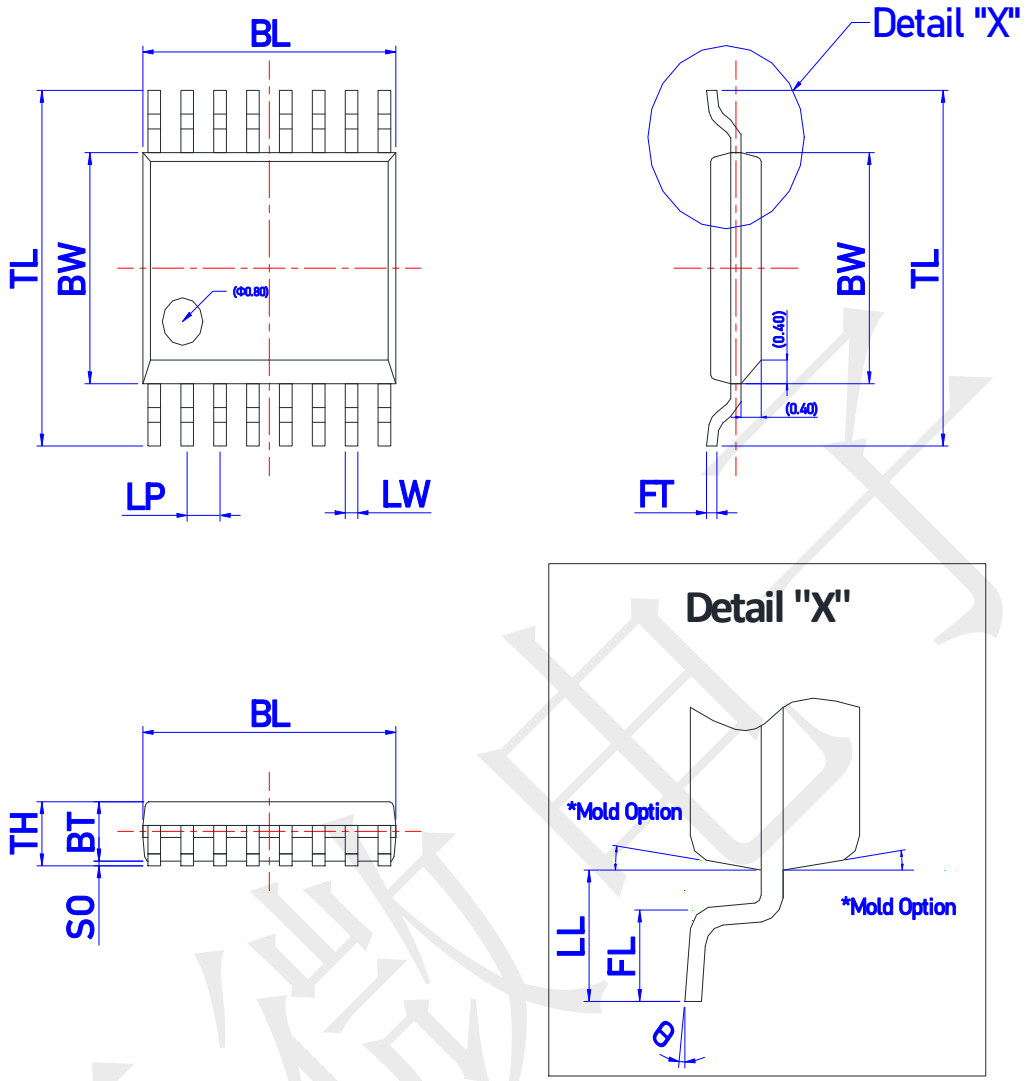
Packaging diagram (SOP16-150)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	10.00 (9.90) 9.80	4.00 (3.90) 3.80	6.20 (6.00) 5.80	0.430 TYP	1.270 TYP	0.250 (0.200) 0.150	1.55 (1.45) 1.25	0.200 (0.150) 0.060	1.650 Max.	1.25 (1.04) 0.80	0.80 (0.60) 0.45	8 (4) 0

Packaging diagram (TSSOP16-150)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	5.05 (5.00) 4.95	4.00 (3.90) 3.80	6.30 (6.00) 5.70	0.250 TYP	0.650 TYP	0.250 (0.200) 0.150	1.05 (1.00) 0.95	0.100 (0.080) 0.020	1.100 Max.	1.25 (1.05) 0.85	0.85 (0.65) 0.40	8 (4) 0

(All specs and applications shown above are subject to change without prior notice.)